ASD INTERIM REPORT 7-865 (IV)
March 1962

SILICON SEMICONDUCTOR NETWORKS MANUFACTURING METHODS

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H. G. Cragon

Texas Instruments Incorporated
Components Division
Dallas, Texas

Contract No. AF 33(600)-42210
ASD Project 7-865

Interim Technical Engineering Report
July-September 1961

Techniques for fabrication, assembly, and application of functional electronic blocks are being established.

Electronics Branch
Manufacturing Technology Laboratory

Aeronautical Systems Division
United States Air Force
Wright-Patterson Air Force Base, Ohio

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Process techniques, manufacturing equipment designs, and assembly techniques for SOLID CIRCUIT* semiconductor networks are being established. Pilot-line equipment has been constructed and is being evaluated and improved.

Effort has been concentrated on developing and refining processes for producing single-chip, planar, oxide-protected devices with evaporated lead interconnections. Emphasis remains strong on doing as much processing as possible on silicon in slice form. This philosophy necessitated further refinements to ensure isolation of components. Several methods of improving isolation are described.

A molecular electronic computer incorporating 587 semiconductor networks has been completed and tested.

*Trademark of Texas Instruments Incorporated.

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FOREWORD

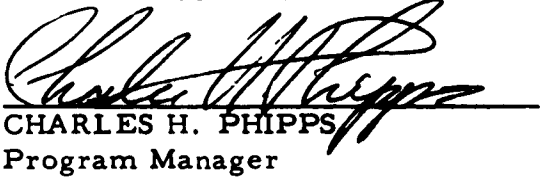
This Interim Technical Progress Report covers the work performed under contract AF 33(600)-42210 from 1 July through 30 September 1961. It is published for technical information only and does not necessarily represent the recommendations, conclusions, or approval of the Air Force.

This contract with the Components Division of Texas Instruments Incorporated was initiated under Manufacturing Methods Project No. 7-865, "Silicon Semiconductor Solid Circuits." It is under the technical direction of Mr. Paul Poliquin of the Electronics Branch, Manufacturing Technology Laboratory, Directorate of Materials and Processes of the Aeronautical Systems Division. Assistance is furnished by Captain Lawrence Roesler, Molecular Electronics Branch, Electronic Technology Laboratory of the Aeronautical Systems Division.

The Manufacturing Methods program and related contracts for research and development, manufacturing techniques, and application of semiconductor networks to equipments are administered by Charles H. Phipps, Program Manager, Semiconductor Networks Department, Texas Instruments Incorporated. The work performed during this report period was under the supervision of Dr. Jay W. Lathrop and William C. Brower, Semiconductor Networks Department, Components Division; and H. G. Cragon, Missile and Space Department, Apparatus Division.

The primary objective of the Air Force Manufacturing Methods Program is to develop new manufacturing techniques and demonstrator equipment, thereby making reliable semiconductor networks (functional electronic blocks/molecular electronics) available in quantity for application to future equipments.

The words "semiconductor networks" are used by Texas Instruments to describe a genus of related products, whereas the terms "functional electronic blocks" and "molecular electronics" are frequently used by the Air Force. The term "SOLID CIRCUIT" is reserved by Texas Instruments as a trademark for this type of product.

Approved by 

CHARLES H. PHIPPS
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Approved by 

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Copies of ASD Technical Reports should not be returned to the Aeronautical Systems Division unless return is required by security considerations, contractual obligations, or notice on a specific document.

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Section I

INTRODUCTION

1.1 Objectives and Scope

The objectives of contract AF 33(600)-42210 are twofold:

a. To establish production processes and techniques for manufacture of semiconductor networks

b. To establish production techniques for the assembly of equipment utilizing semiconductor networks.

The semiconductor networks fabricated under this program are representative of the current state of the art, and capable of performing a variety of circuit functions. This program is complementary to the investigations of design techniques for semiconductor networks under contract number AF 33(616)-6600, connection techniques under contract number AF 33(616)-8133, and several programs for the design of specific semiconductor networks.

1.2 Program Status

During the reporting period, particular emphasis was placed on fabrication of semiconductor networks for the prototype computer, and construction and testing of this computer.

Process development continues to emphasize techniques that will allow processing the semiconductor material to the greatest possible extent in slice form. Consequently, production equipment design and fabrication has progressed furthest in preparation of materials, diffusion, photolithography, and lead deposition. Requirements for the remaining process equipment have been defined, and design, if required, initiated.

This program is current with schedule requirements, and there is a high degree of confidence that the implementation of the pilot-line facility will be successful.

Section II

PROCESS STUDIES

2.1 General

In the first and second quarterly reporting periods, processing studies were directed at determining optimum device designs from a reliability and manufacturing standpoint. It was determined during this period that the functional electronic blocks would be single-chip, planar, oxide-protected devices, with evaporated lead interconnections. The electrical feasibility of such devices was proven. The effort during the third quarterly reporting period was directed at developing and refining the processes for producing such configurations. From a manufacturing-cost point of view it was important to do as much of the processing in slice form as possible. This was the principal consideration in guiding the process studies.

2.2 Preparation of Materials

2.2.1 Chemical Polishing

Investigations of chemical polishing techniques were directed toward solving several problems which had arisen since the introduction of this method into production. The following were the principal problems.

a. Chemically polished slices were rounded at the edges and thicker in the center. Measurements taken of total slice thickness using a dial micrometer showed that slices were 1.8 mils thicker in the center (average) than at a point 1/8 inch from the edge. This difference was similar for slices with diameters of 7/8 inch and 1-1/4 inches. Curvature of the silicon surface would make it difficult to obtain sharp images over the entire slice using glass photomasks.

b. Surfaces of the slices appeared wavy or uneven without magnification. This effect seemed to be caused by nonuniform etching due to etch turbulence in the holding fixture.

c. A haze frequently appeared on the slices, usually worse at the edges. The haze was most easily observed under low-angle illumination from the intense beam of a microscope light. In some cases, the haze could be washed off by careful cleaning, but in most cases, it could not be removed and had the appearance of clouds of microscopic etch pits. The haze was attributed to improper quenching of the etch action.

d. Reproducibility and production rates were both low, which indicates the need for mechanization of this operation.

Improved Etch-Polish Fixture
Figure 1

An examination of the existing etch-polishing machine described in ASD Interim Report 7-865 (III) indicated that most of the difficulties were related to the method of holding the slices in the fixture.

The old etch-polish fixture consisted of three flat Teflon discs, 1/4-inch thick and 5 inches in diameter, separated about 1/4 inch by Teflon pins pressed through the discs. The pins also provided the means by which the slices were held by forming a circular "cage." The three discs were suspended by a Teflon shaft from the reversing motor, which provided the motion in the etch. This holder was lowered into the etch container and rotated approximately five revolutions, reversed, etc. The quenching was done by dilution with deionized water.

Confinement of the slices in the holder apparently was responsible for uneven etching, slice rounding, and slow quenching. To provide freer motion during the operation, a polyethylene basket was designed, 5 inches in diameter and 2 inches high, with a removable cover. It is shown in Figure 1. The walls of this basket are perforated with 3/8-inch and 1/2-inch holes, which allow greatly increased etch agitation and circulation around the slices. Cushioning action of the liquid prevents breakage or scratching, and rapid agitation keeps the slices from sticking together. Agitation is provided from a central shaft by a 72-rpm "Slosyn" motor which oscillates the cage 1/3 of a revolution in opposite directions under the control of adjustable timer switches.

It was found that rapid quenching was necessary to eliminate staining and haze. Addition of a minimum of three times the etch volume of deionized water in less than 2 seconds is required. Quenching was performed experimentally by pouring containers of deionized water into the etch container. In production, a water-storage and discharge system would be used.

Results obtained are summarized below:

Table 1. Comparison of Old and New Etch-Polish Methods

Item	New Method	Old Method
Polish output (total)	200 slices per hour	Approximately 20 slices per hour
Polish yield (good slices)	Better than 99 percent	Approximately 80 to 85 percent
Thickness difference from center to edge	0.5 to 0.8 mil (Thickness does not vary with slice diameter.)	1.4 to 2.4 mils
Staining	No stain. (Some slices have a slight haze, but there is no evidence that this is detrimental.)	About 90 percent were stained

Table 1. Comparison of Old and New Etch-Polish Methods (Continued)

Item	New Method	Old Method
Cost of planar etch	About 2.5 cents per good slice (assuming a 99 percent yield).	About 15.5 cents per good slice (assuming an 80 percent yield).

2.3 Diffusion

2.3.1 General

One of the biggest problems in fabricating multiple devices on a single piece of silicon is in obtaining isolation of the various components. Much of the work described in this section is directed at developing methods of isolation which still allow optimization of the electrical characteristics of the devices. At least four possibilities for isolation are possible:

a. Diffusion Through The Slice

In this technique, the wafer is masked on one face, unmasked on the other and diffused with a conductivity type opposite to that of the bulk. An advantage of this technique is that homogeneous collector material is used, simplifying diffusion control. A disadvantage is the necessity of working with thin slices or long diffusion times.

b. Diffusion Through an Epitaxial Layer

This technique is similar to "a" but requires shorter diffusion time to get through the relatively thin (approximately 0.5-mil) epitaxial layer. The epitaxial layer must be of conductivity type opposite to that of the substrate. The disadvantages are the extra degree of control required on the layer and the relatively high cost of the material.

c. Triple Diffusion

In this method, the collector region is diffused as well as the base and emitter. An advantage is that low-cost material is used, but the disadvantage is that control of the base diffusion is more critical when diffusing into an already-diffused layer.

d. Gold Diffusion

Here the devices are fabricated by triple diffusion on relatively highly-resistivity (approximately 20 ohm-cm) material and then, by subsequent gold diffusion, the substrate is converted to intrinsic material. The advantage of this method lies in the improved

ac isolation through elimination of the PN junction capacitance. The disadvantage is the additional control required for gold diffusion.

Isolation has been achieved by all of the above methods, but most of the device work has been concentrated on method c.

It is apparent that all isolation methods, and particularly c., call for a considerable degree of control of the diffusion process. If any real degree of diffusion control is to be realized, it is necessary to understand the parameters affecting diffusion and particularly the interactions at the surface. Basic to the study of diffusion is an adequate method of determining the concentration profile of diffused layers.

2.3.2 Diffusion Profile Study

A method of determining diffusion profiles rapidly and accurately has been developed by successively removing plane decrements of known thickness by chemical etching and measuring the resulting sheet resistivity.

Decrements of silicon are removed with 1 HF, 60 HNO_3, 20 HA_c (etch rate is a few tenths of a micron per minute). The thickness of each decrement is found by dividing the junction depth, which is known from independent measurement, by the number of decrements removed to reach the junction, keeping the etch time constant. The location of the junction is identified by a sharp drop in sheet resistivity. Since the etch rate is continuously monitored in this way, small fluctuations in etch composition do not introduce errors. For a given etch time, larger or smaller decrements can be removed by varying the HF concentration.

Experiments on the etching of P-type bulk material have shown the etch rate to be independent of resistivity for etches of low HF concentration. This can be explained by an etch rate in this region limited by the HF dissolution of silicon oxide[1] –a phenomenon that does not depend on the electrical properties of the silicon.

An ac resistivity test set is used to measure sheet resistivity. The slice is indexed with the probe to ensure that sheet resistivity is always measured at the same spot.

Sheet conductivity is plotted as a function of the total thickness of silicon removed. The derivative of this curve at any point is the conductivity at that point. The differentiation is performed graphically.

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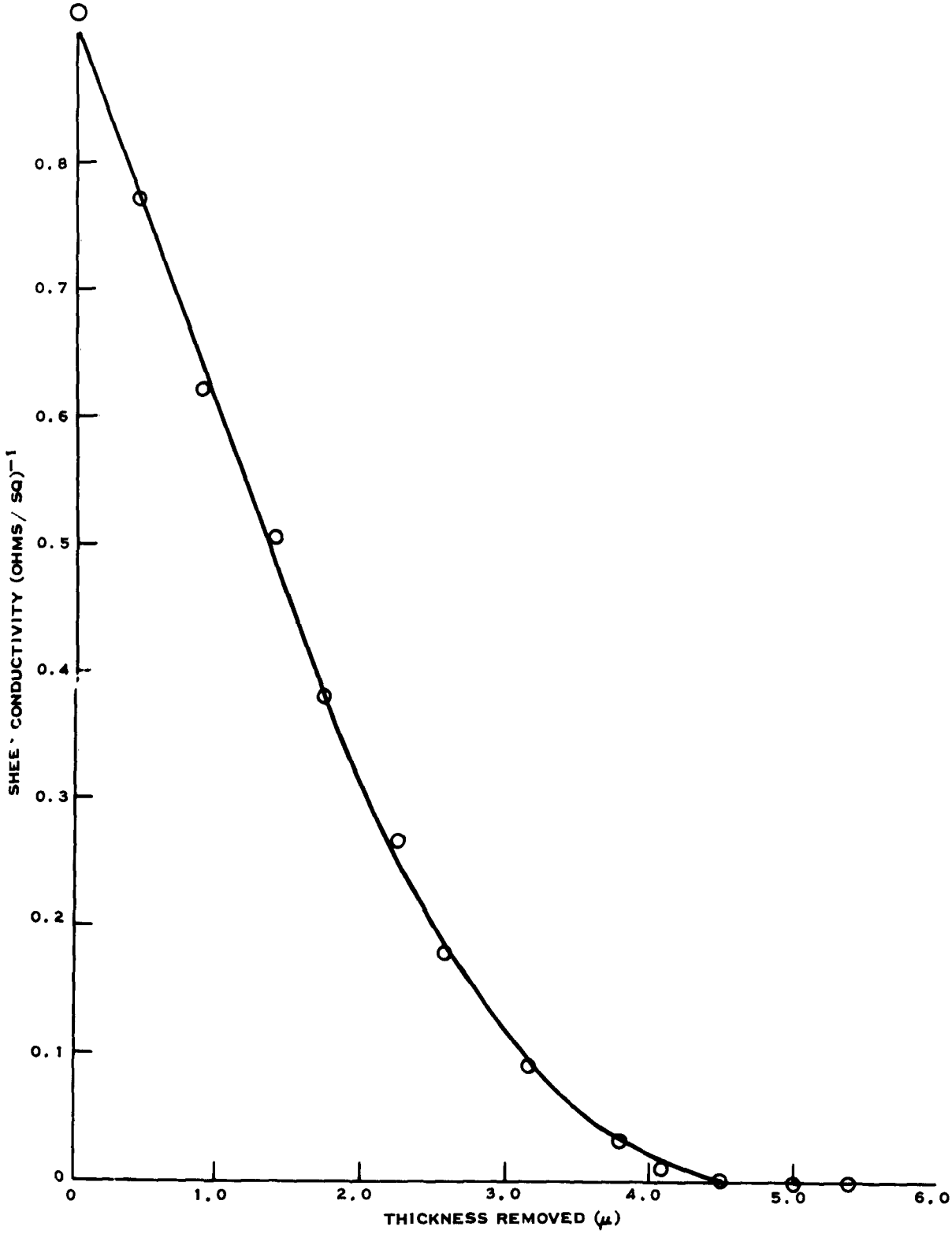
[1] Robbins, H. and Schwartz, B., Journal of the Electrochemical Society 107, pp. 108-111.



Sheet Conductivity Vs. Thickness of Silicon Removed (Phosphorus Diffusion)
Figure 2

The concentration is deduced from the conductivity using Irvin's data.[2]

Table 2 presents the experimental data for a typical phosphorus emitter diffusion. Figure 2 is a plot of sheet conductivity Vs. distance. Figure 3 shows the derived curve, N_x Vs. X, for this diffusion. This curve is similar to those published for high-concentration phosphorus diffusion.[3,4]

Table 2. Sheet Resistivity Vs. Thickness of Silicon Removed (Phosphorus Diffusion)

$X_j = 5.6\ \mu$

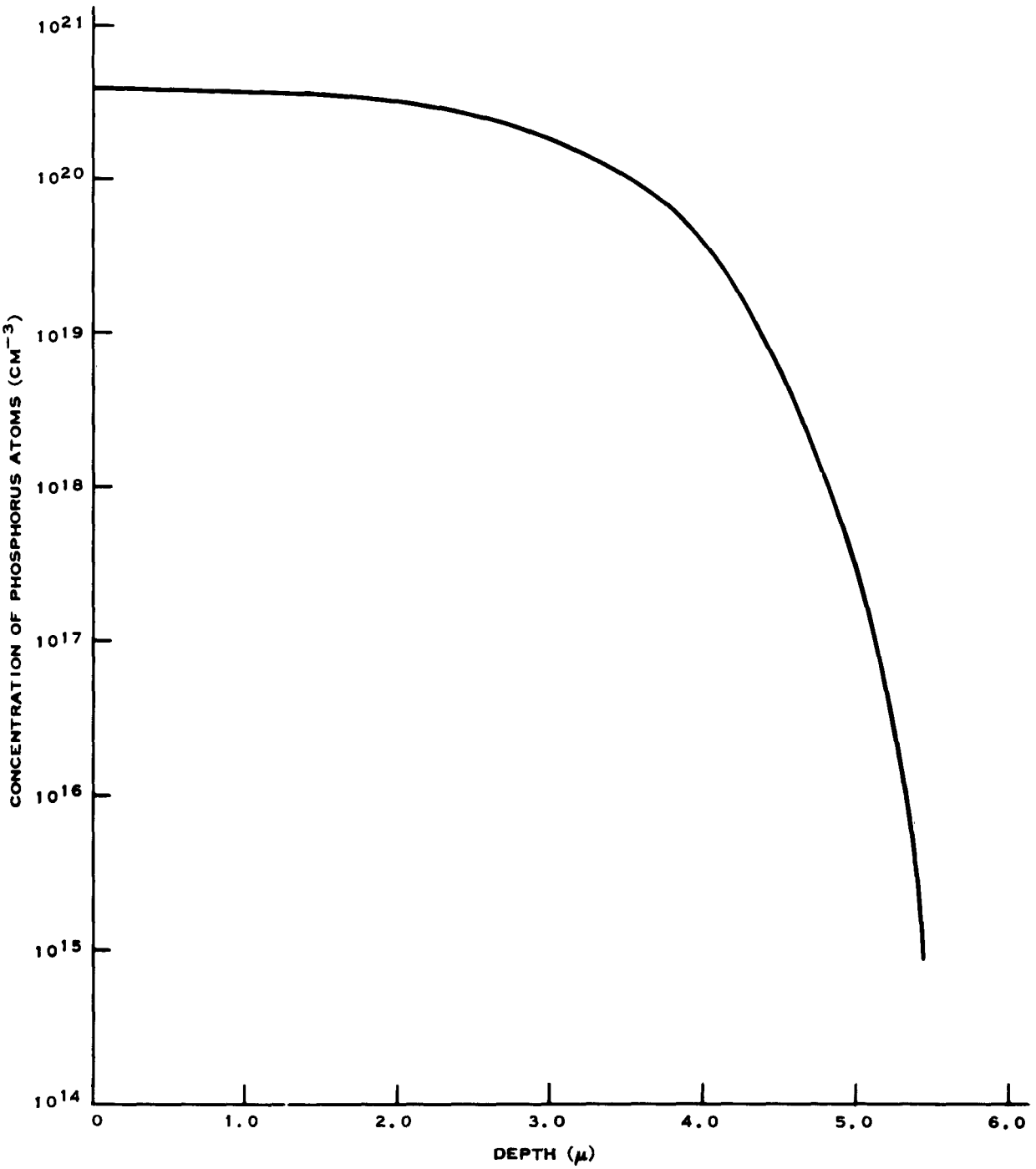
$\rho_o = 10$ ohm-cm

Step	ρ_s (ohms/sq)	σ_s (ohms/sq)	X (μ)
0	1.1	0.83	0
1	1.3	0.77	0.45
2	1.6	0.62	0.90
3	1.6	0.50	1.4
4	2.6	0.38	1.8
5	3.6	0.28	2.3
6	5.8	0.17	2.7
7	12.0	0.083	3.2
8	30.0	0.033	3.6
9	100.0	0.010	4.1
10	420.0	0.0024	4.5
11	1500.0	0.0067	5.0
12	>3000.0		5.4
13	400.0		5.7

[2] Irvin, J., Unpublished results distributed by Ron Wackwitz.

[3] Tannenbaum, E., Solid State Electronics, 2, pp. 123-132.

[4] Subashiev, V.K., Landsman, A.P., and Kukharskii, A.A., Soviet Physics–Solid State, 2, pp. 2406-2411.



Phosphorus Concentration Vs. Depth
Figure 3

Table 3 presents the experimental data for a typical two-step boron base diffusion. Figure 4 is a plot of sheet conductivity Vs. distance. Figure 5 is the derived curve, N_x Vs. X. A diffusion of this sort, where the diffusion length of the second step is much greater than the diffusion length of the first step, with surface insulated during the second step, should give a Gaussian distribution of diffused impurity.[5] Fitting a Gaussian distribution to the deeper points of Table 3 gives a surface concentration an order of magnitude higher than the experimental value at the surface.

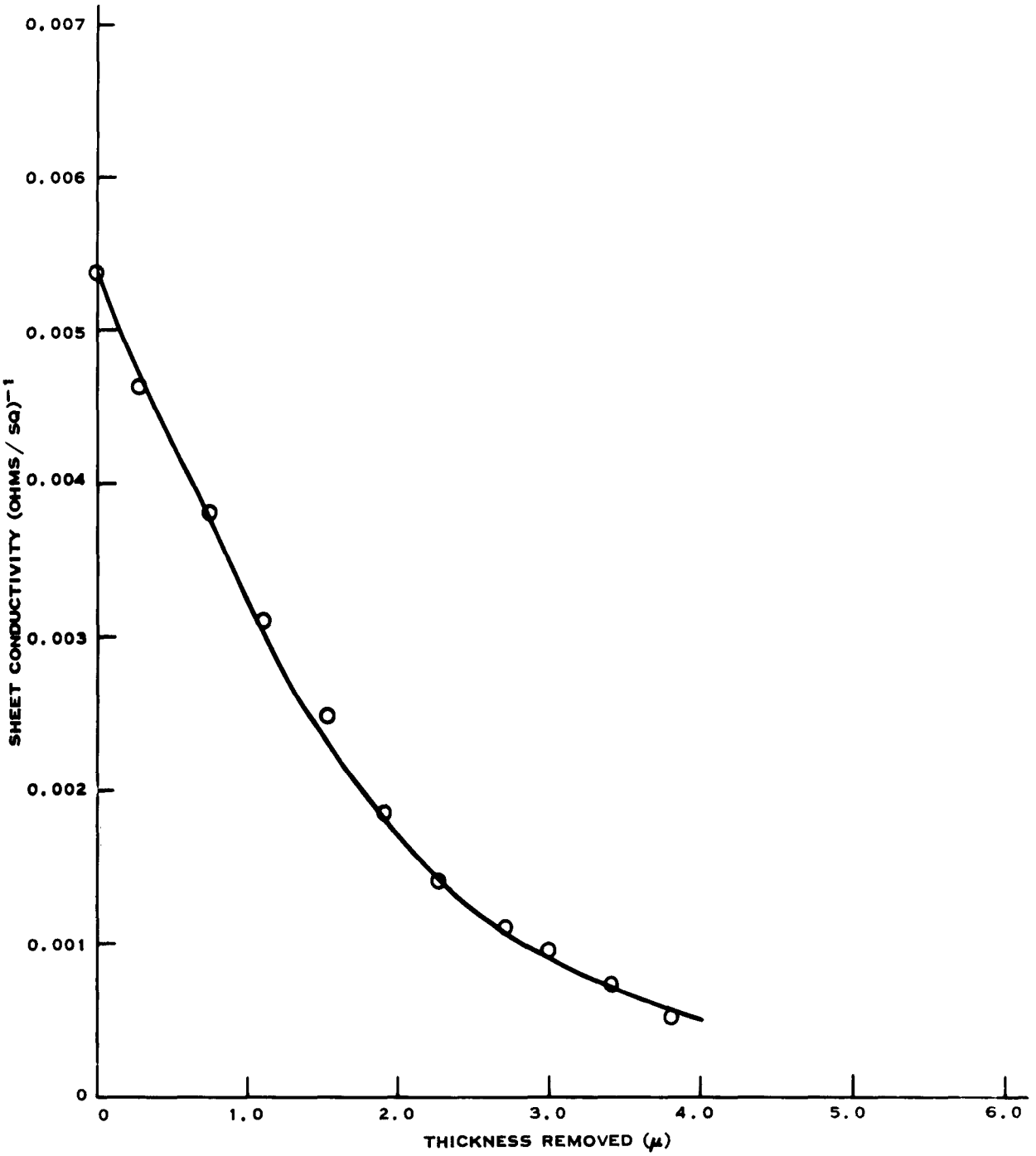
Table 3. Sheet Resistivity Vs. Thickness of Silicon Removed (Boron Diffusion)

$X_j = 5.4\ \mu$

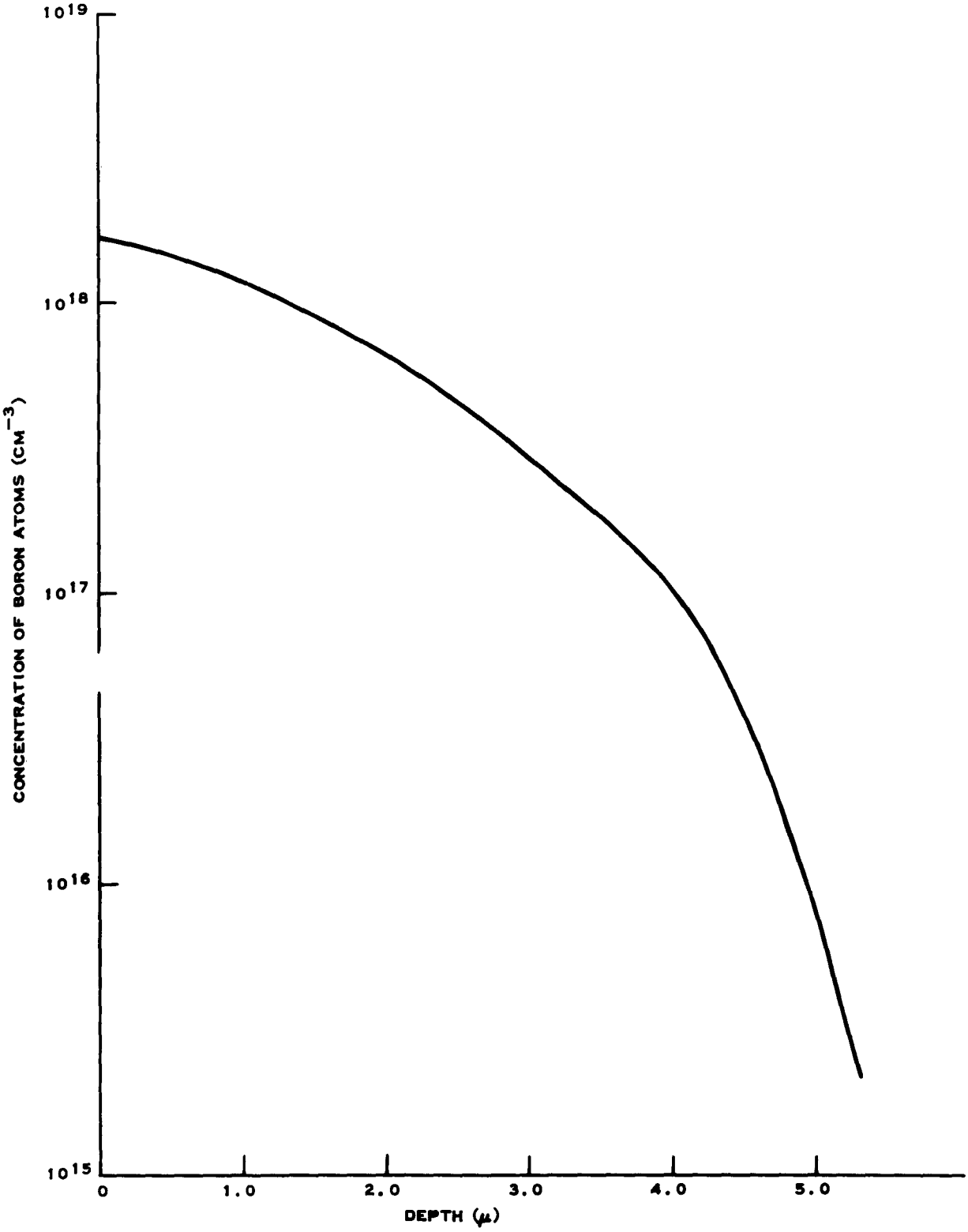
$\rho_o = 3$ ohm-cm

Step	ρ_s (ohms/sq)	σ_s (ohms/sq)	X (μ)
0	190	0.0053	0
1	220	0.0045	0.38
2	260	0.0038	0.76
3	320	0.0031	1.1
4	400	0.0025	1.5
5	520	0.0015	1.9
6	700	0.0014	2.3
7	820	0.0011	2.7
8	1100	0.0091	3.0
9	1500	0.00067	3.4
10	2100	0.00048	3.8
11	>3000		4.2
12	>3000		4.6
13	>3000		4.5
14	>3000		5.3
15	250		5.7

[5] Wackwitz, R. C., Memo to R. L. Petritz and A. E. Sobey, Jr., 8 August 1961, p. 8.



Sheet Conductivity Vs. Thickness of Silicon Removed
(Boron Diffusion)
Figure 4



Boron Concentration Vs. Depth
Figure 5

2.3.3 Boron Loss at Interface

As a direct result of these profiling experiments, it can be concluded that a great deal of boron is lost in growing the oxide layer, i.e., the surface may not be considered as insulated. To exercise control then, one must control the oxidation very closely during diffusion, particularly during the first part of the diffusion.

To further verify this, an experiment was run in which chemically polished, 2-5 ohm-cm, N-type slices were given a 60-minute boron deposition at 900°C. Trimethyl borate was used as a source of diffusant. The slices were cleaned in a boron glass solvent after deposition and diffused for 200 minutes at 1200°C in different atmospheres. The experimental conditions for the oxidation step and the resulting surface concentrations are given in Table 4.

Table 4. Experimental Conditions for Oxidation and Resulting Surface Concentrations

Sample	Atmosphere	Surface Concentration
1	Dry N_2	2.0×10^{19}
2	SiO_2 deposited, dry N_2	2.0×10^{19}
3	Wet N_2	5.3×10^{18}
4	Steam	4.5×10^{17}

The oxide film on sample 2 was pyrolytically deposited at a relatively low temperature (about 700°C). The wet nitrogen used for sample 3 was saturated with water at room temperature.

The impurity concentration profiles[6] for samples 1 and 4, shown in Figure 6, illustrate graphically the importance of considering the effects of different oxidizing conditions.

Samples 1 and 2 had identical surface concentrations. If the loss of boron during oxidation were due to a segregation phenomenon at the Si-SiO_2 interface, sample 2 should have had a lower surface concentration. As there was no difference in surface concentration, it was assumed that the loss of boron is due solely to the "trapping" of boron atoms in the growing oxide film. On the basis of this assumption, an equation relating the oxidizing and diffusing conditions of the second step to the loss of boron has been derived.

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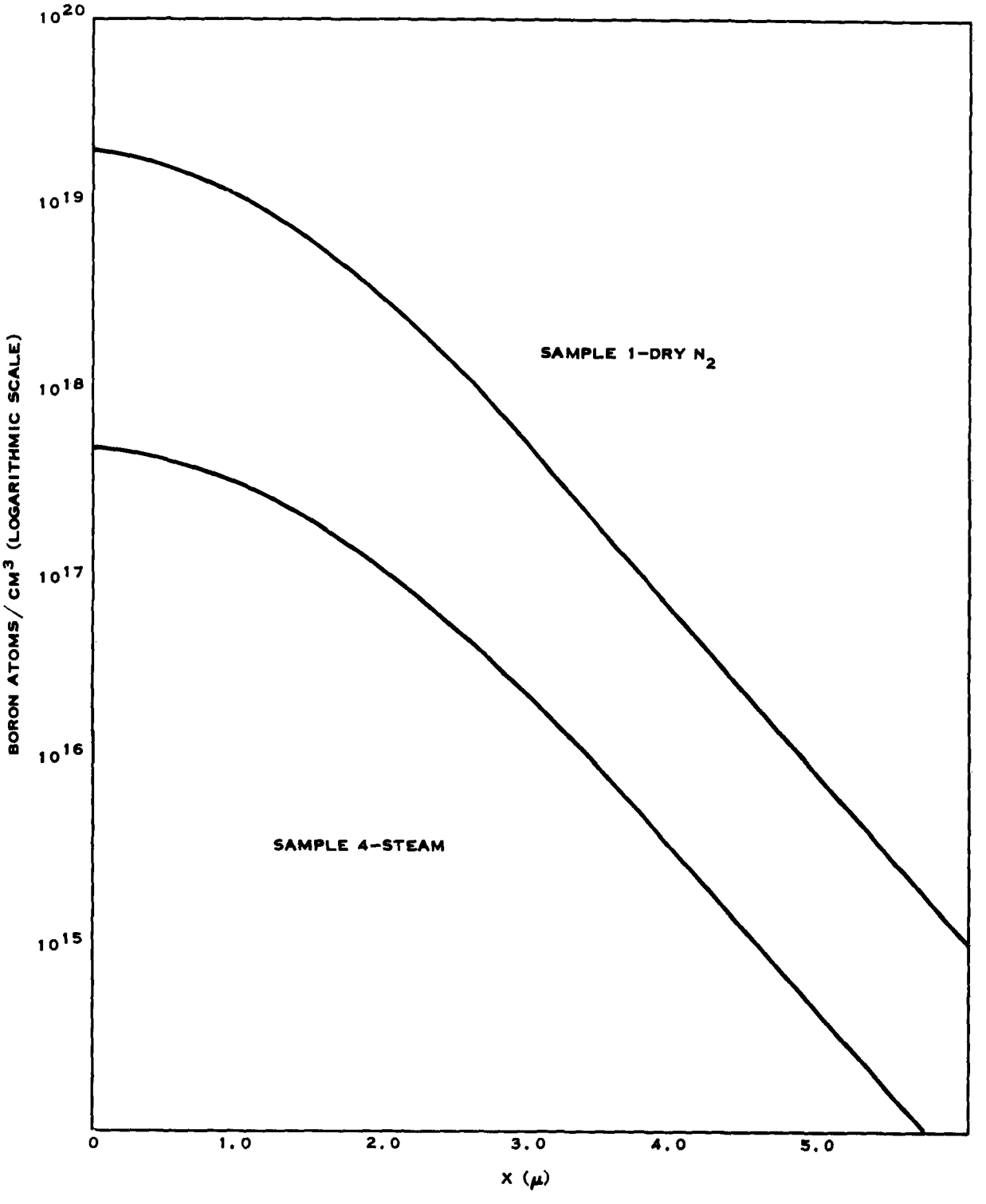
[6] R. Harris, Texas Instruments Technical Report No. 03-61-77, 11 September 1961.



Boron Concentration for Different Oxidizing Atmospheres
Figure 6

An expression relating the surface concentration of a two-step diffusion to the diffusion conditions for the case of an insulated (no boron lost) interface has been previously reported.[7] For this special case,

$$N_{s2} = \frac{2}{\pi} \frac{\sqrt{D_1 t_1}}{\sqrt{D_2 t_2}} N_{s1} \tag{1}$$

where subscript 1 refers to the first step and subscript 2 refers to the second step. Equation (1) was derived by equating Q_1, the number of atoms per square centimeter introduced during the first step, to Q_2, the number of atoms per square centimeter present after the second step. It can be shown that, using the above expression for surface concentration, the diffused impurity distribution may be written

$$N_x = \frac{2}{\pi} \frac{\sqrt{D_1 t_1}}{\sqrt{D_2 t_2}} N_{s1} \left[e^{-\frac{x^2}{4 D_2 t_2}} \right] \tag{2}$$

for the insulated boundary case.

Assuming the distribution of diffused impurity given by Equation (2) and a parabolic oxide growth described by

$$a^2 = Kt, \tag{3}$$

the number of boron atoms lost per square centimeter during the oxidation, Q_L, can be determined. Knowing Q_1 and Q_L, Q_2 can be determined. From Q_2 one can find an expression for N_{s2} taking into account the boron lost during the oxidation. This new expression for N_{s2} is

$$N_{s2} = \frac{2}{\pi} \frac{\sqrt{D_1 t_1}}{\sqrt{D_2 t_2}} N_{s1} \left(1 - \frac{0.44}{2\pi} \sqrt{\frac{K}{D^2}} \, 1nt_2 \right) \tag{4}$$

The experimental data presented in Table 4 can be used to check Equation (4). To use Equation (4), it is necessary to have values for the oxidation parameter, K, in the relation $a^2 = Kt$ for oxidation in steam and in wet nitrogen at 1200°C. Data taken for oxidation in wet nitrogen

[7] ASD Interim Report 7-865 (I), May 1961.

at 1100°C was converted to 1200°C using an activation energy of 1.1 ev.[8] The values calculated for 1200°C are:

$$K = 1.3 \times 10^{-12} \text{ cm}^2/\text{sec (steam)},$$

and

$$K = 8.8 \times 10^{-14} \text{ cm}^2/\text{sec (wet } N_2).$$

A value of 2.0×10^{-12} cm^2/sec was used for the diffusion coefficient of boron at 1200°C. Table 5 compares calculated ratios of concentrations to the measured ratios.

Table 5. Calculated and Measured Concentration Ratios

Ratio	Calculated	Measured
$\frac{N_{s2} \text{ (Sample 1)}}{N_{s2} \text{ (Sample 3)}}$ =	1.3	3.8
$\frac{N_{s2} \text{ (Sample 3)}}{N_{s2} \text{ (Sample 4)}}$ =	9.4	12

An additional test was run in which a slice was deposited at 900°C for 60 minutes. After deposition, the slice was cleaned in the usual manner and scribed into quarters. At this point, each of the four quarter slices has received the same treatments. Then each quarter slice was diffused at 1200°C for 120 minutes under different ambient conditions. These are presented in Table 6.

Table 6. Ambient Diffusion Conditions

No. 1—10 minutes dry N_2 110 minutes wet N_2

No. 2—120 minutes wet N_2

No. 3—60 minutes wet N_2, 60 minutes steam

No. 4—120 minutes steam

This data conforms somewhat better to the theory. The values of K for steam and wet nitrogen are the same as before. A relationship for N_{s2} for the case of oxidation for time t_a under conditions described

[8] Thurston, M., et al, Ohio State University Research Foundation, Seventh Quarterly Technical Report under Contract DA-36-039-56-83874, 31 October 1960.

by K_1 -and then for time $t_b = mt_a$ under oxidation conditions described by K_2 -is

$$N_{s2} = \frac{2}{\pi} \frac{\sqrt{D_1 t_1}}{\sqrt{D_2 t_2}} \left(N_{s1}\, 1 - \frac{0.44}{2\sqrt{\pi}\sqrt{D_2}} \sqrt{K_1}\, \ln t_a + \sqrt{K_2 (m - \frac{K_1}{K_2})}\, \ln(m+1) \right) \quad (5)$$

Table 7 compares the ratio of surface concentrations predicted by Equation (5) to the measured ratios.

Table 7. Calculated and Measured Ratios of Surface Concentrations

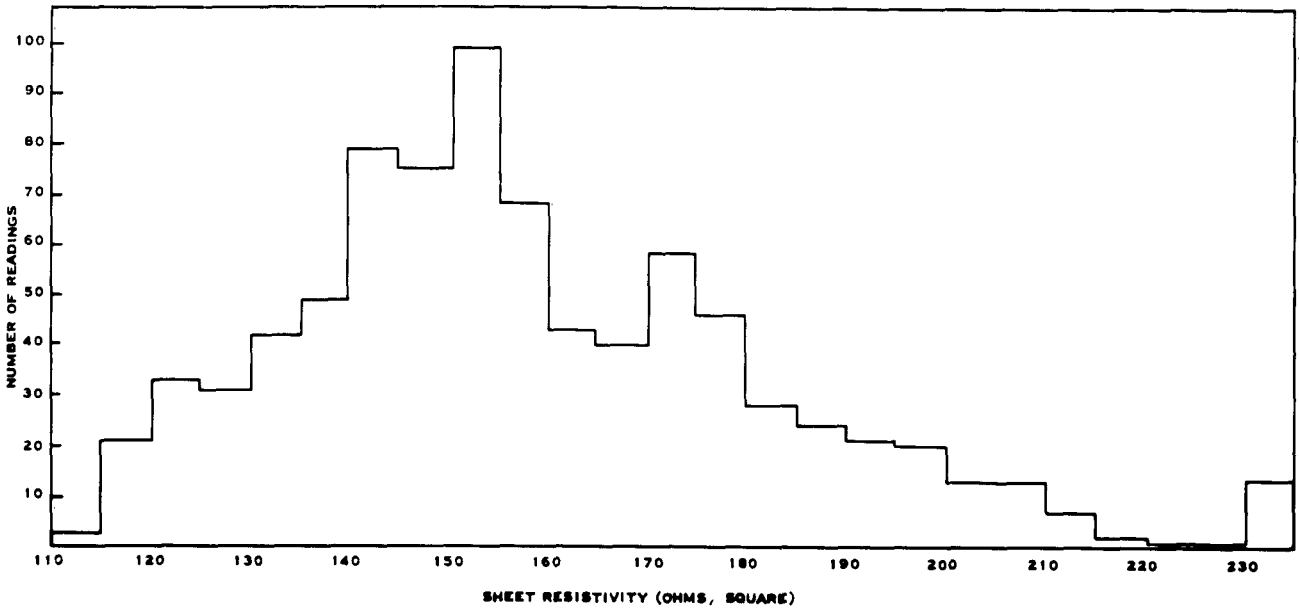
Ratio	Calculated	Measured
$\frac{N_{s2}\ (\text{Sample 1})}{N_{s2}\ (\text{Sample 2})} =$	1.0	1.0
$\frac{N_{s2}\ (\text{Sample 2})}{N_{s2}\ (\text{Sample 3})} =$	1.1	1.5
$\frac{N_{s2}\ (\text{Sample 3})}{N_{s2}\ (\text{Sample 4})} =$	5.4	5.5

This theory therefore shows fair agreement with experiment. Knowledge of the way in which diffusion and oxidation compete for the boron as quantitatively stated in Equation (4) and (5) allows diffusion and oxidation conditions to be more intelligently determined.

2.3.4 Reproducibility Data

Having established the importance of controlling the oxidation rate during diffusion, a test was instituted to determine the degree of reproducibility during boron base diffusions in which the conditions were controlled as closely as possible. The test consisted of nine runs made over a period of six weeks. All runs were identical, inasmuch as they were within specifications set in production. Each run contained five slices. From these five slices, 100 sheet-resistivity measurements were taken using both sides of each slice.

Figure 7 is a bar graph of the sheet resistivity distribution in increments of 5 ohms per square. The test indicated that 84 percent of the resistivity readings were within ±20 percent of the mean, and that 54.5 percent of the resistivity readings were within ±10 percent of the mean.



Sheet Resistivity Distribution
Figure 7

These results indicate only the reproducibility of methyl borate and a test of the same type must be made using phosphorus.

2.3.5 Gold Diffusion

2.3.5.1 General

Gold is used in semiconductor networks to kill minority carrier lifetime, thus reducing the reverse recovery time in diodes and transistors. As indicated in the last quarterly report, gold may also be used to convert silicon to intrinsic resistivity, thereby achieving isolation without using PN junctions.

In order to investigate these phenomena, a technique for repeatedly introducing controlled amounts of gold is necessary. A two-step diffusion procedure has been developed for uniform doping of silicon slices with gold.

An excess of gold is vacuum-deposited on the back of a silicon slice. The slice is then subjected to a first diffusion for a time, t_1, at a temperature of T_1 (with diffusion coefficient D_1). Diffusions have

been made in a quartz system with an air atmosphere. The number of gold atoms introduced, Q_1, is

$$Q_1 = N_{s1} \int_{x=0}^{x=\infty} \operatorname{erfc} \frac{x}{2\sqrt{D_1 t_1}}$$

$$= \frac{2}{\pi} N_{s1} \sqrt{D_1 t_1} \text{ atoms/cm}^2 \qquad (6)$$

where N_{s1} is the solid solubility of gold in silicon at temperature T_1. The numerical solution below shows that the error from assuming a semi-infinite slice for the integration is not important.

The excess gold is removed from the back of the slice with aqua regia and the slice is subjected to a second diffusion at temperature T_2 and time t_2 sufficient to distribute the gold throughout the slice uniformly. For convenience, T_2 is chosen equal to T_1 and one furnace is used for both steps. The numerical solution below shows that a t_2 of 30 minutes is sufficient for concentrations and thicknesses of interest. Since only the gold introduced during the first step is present, the uniform bulk concentration, N_{Au}, can be found.

$$N_{Au} L = Q_1 \text{ atoms/cm}^2$$

$$N_{Au} = \frac{2N_{s1}}{L} \sqrt{\frac{D_1 t_1}{\pi}} \text{ atoms/cm}^3 \qquad (7)$$

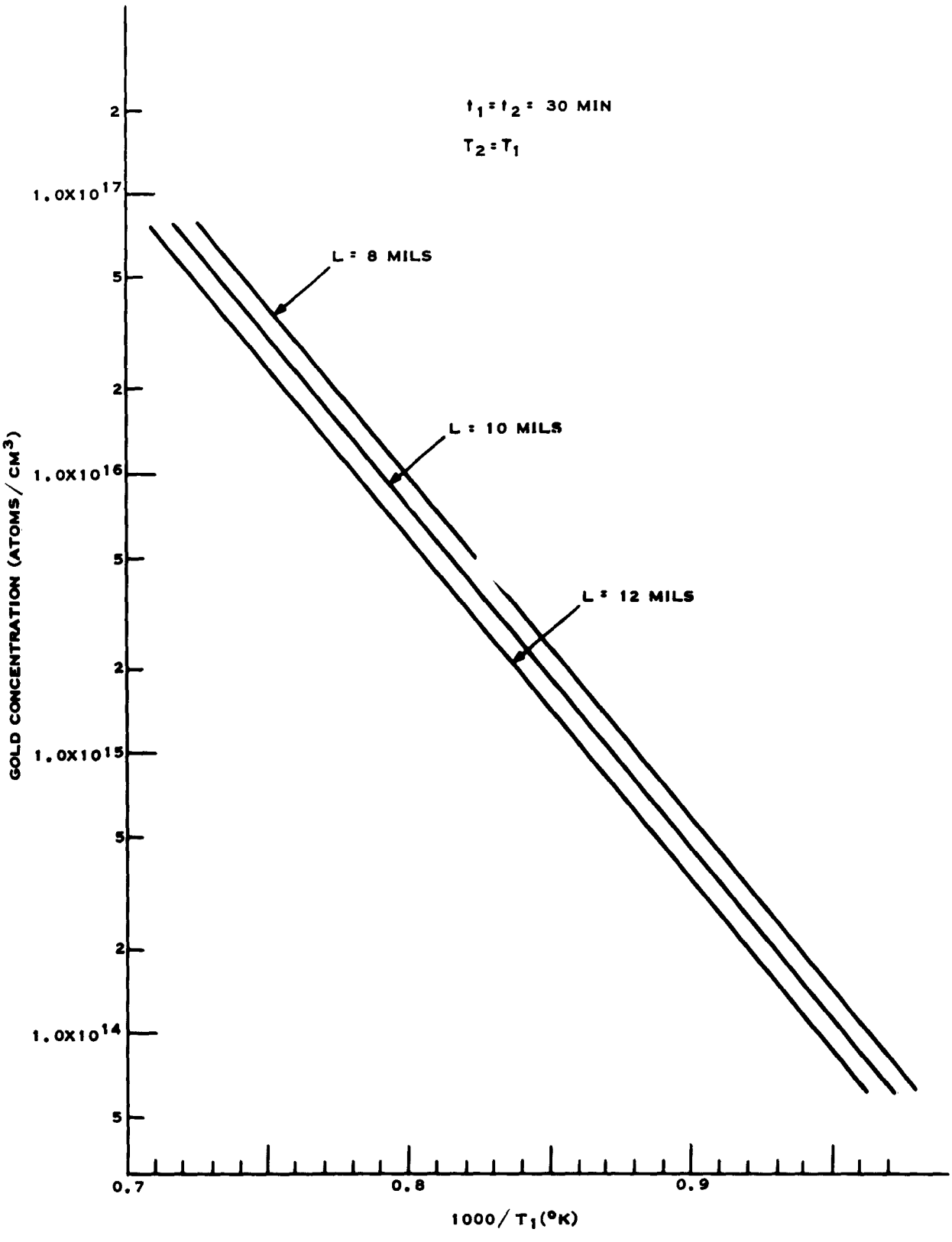
where L is the thickness of the slice.

Using Equation (7) with data for the solid solubility and diffusion coefficient, a family of curves N_{Au} Vs. T_1 for constant t_1 and various L was drawn. These curves are shown as Figure 8. t_1 and t_2 are held constant at 30 minutes. $T_2 = T_1$.

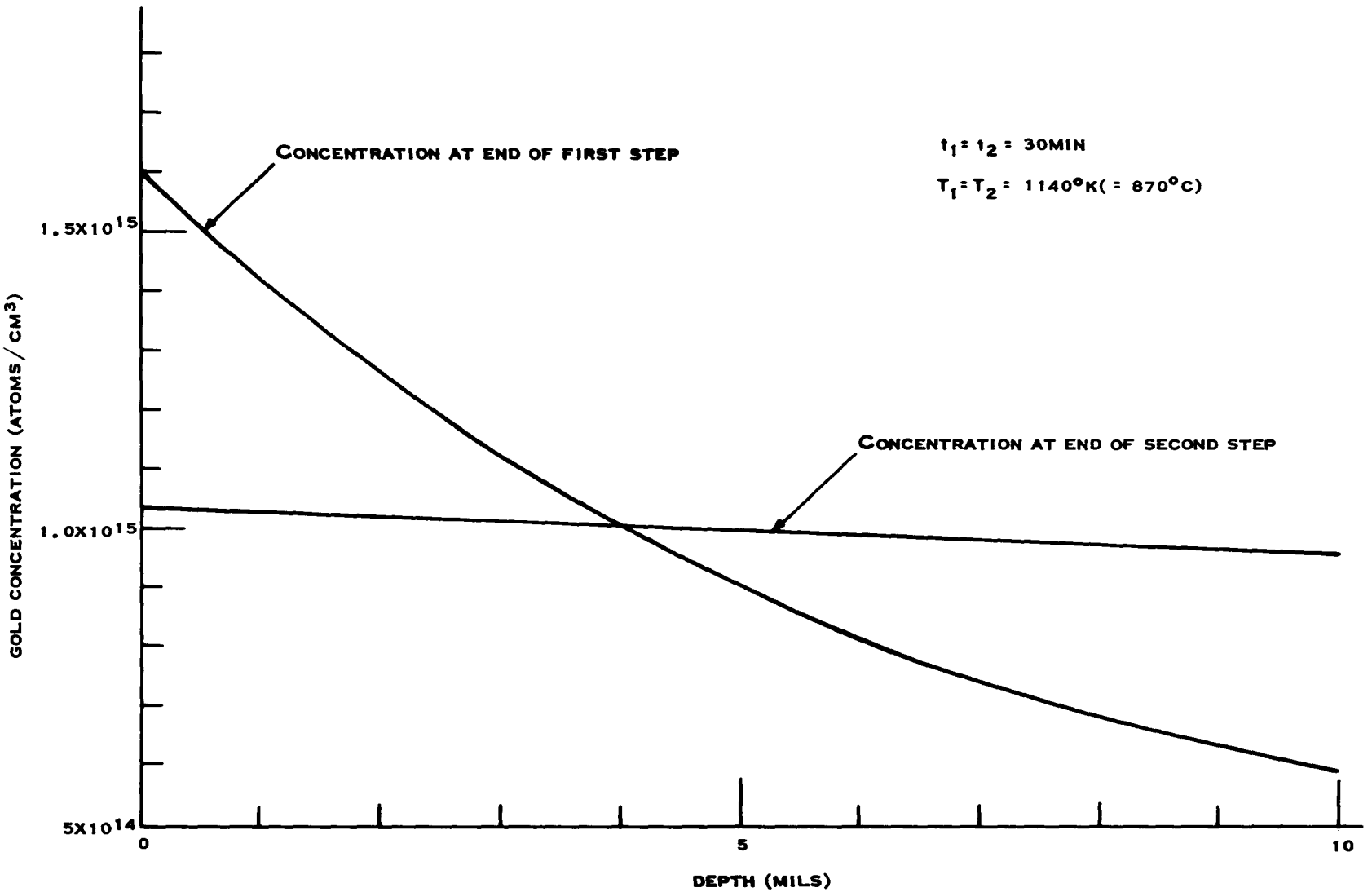
It is possible to solve the boundary-value problem of the diffusion of gold in silicon numerically.[9] Figure 9 shows the calculated gold distribution after the first and second steps of a typical diffusion. The conditions for this diffusion were chosen from Figure 8 to make $N_{Au} = 1.0 \times 10^{15}$ atoms/cm^3.

The nearly constant concentration profile shows that making $T_2 = T_1$ and $t_2 = 30$ minutes is sufficient. The close agreement of the

[9] H.S. Carslaw and J.C. Jaeger, "Conduction of Heat in Solids," Oxford University Press, 466-476, (1959).



Gold Concentration Vs. $1000/T_1$
Figure 8



Concentration Profiles During Gold Diffusion
Figure 9

calculated doping level with that predicted by Figure 8 shows that the error introduced by assuming a semi-infinite slice for the analytic treatment is not important.

2.3.5.2 Use of Gold to Decrease Storage Time

Using this two-step technique, a number of MPRT test transistors were gold-diffused to determine the effect on storage time.

Diffusion controls were adjusted to introduce the following amounts of gold.

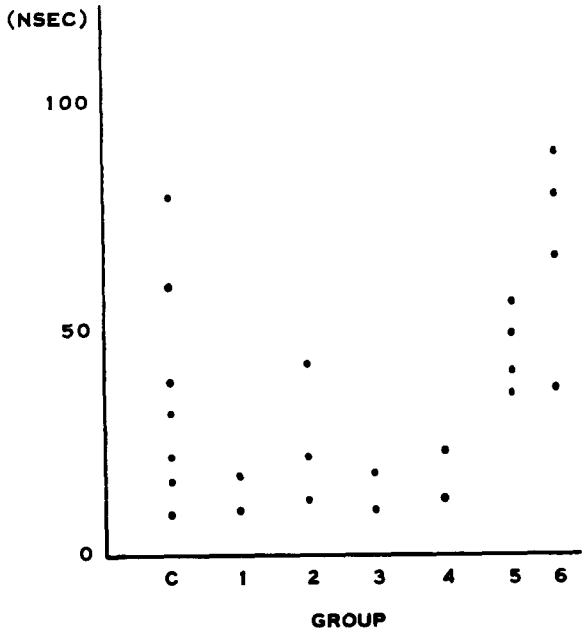
Table 8. Gold Diffusion Levels

Sample Number	Atoms of Au/cm^3
Control	0
1	2×10^{14}
2	4×10^{14}
3	1×10^{15}
4	2×10^{15}
5	7×10^{15}
6	1.5×10^{16}

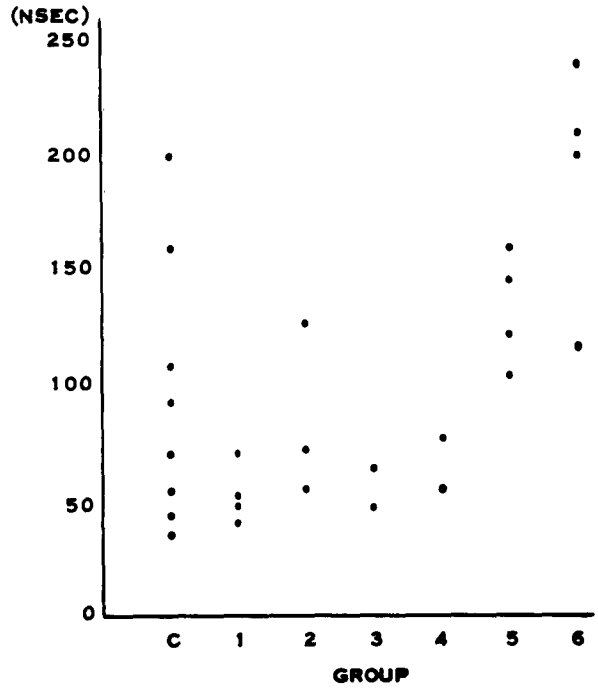
All but a small portion of the excess gold was removed between steps. Because of this excess, the tabulated concentrations are given as minimum values and the spread in gold concentration is probably less than the figures indicate.

All six gold-diffused groups displayed considerably lower storage times than the controls, although the R_{cs} was somewhat higher, particularly in groups 5 and 6. There was also apparently some decrease in the delay, rise, and fall times of groups 1, 2, 3, and 4 and some increase in these times for groups 5 and 6. This last result was manifest only as an ill-defined trend, however, and should not be considered conclusive.

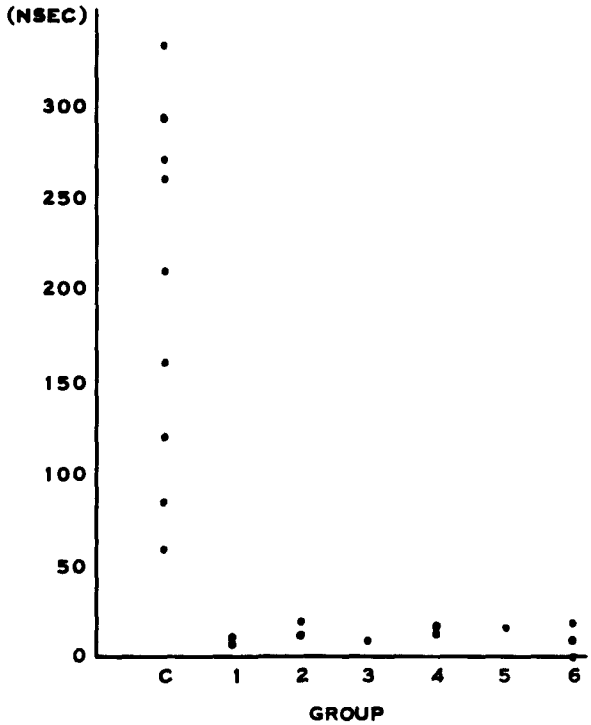
Switching times are presented in Table 9 and in Figures 10 through 14. The small number of samples in some of the groups resulted from fabrication difficulties encountered after diffusion. This investigation will be continued, and in future tests, the complete removal of excess gold will be accomplished by lapping several tenths of a mil from the back of each slice.



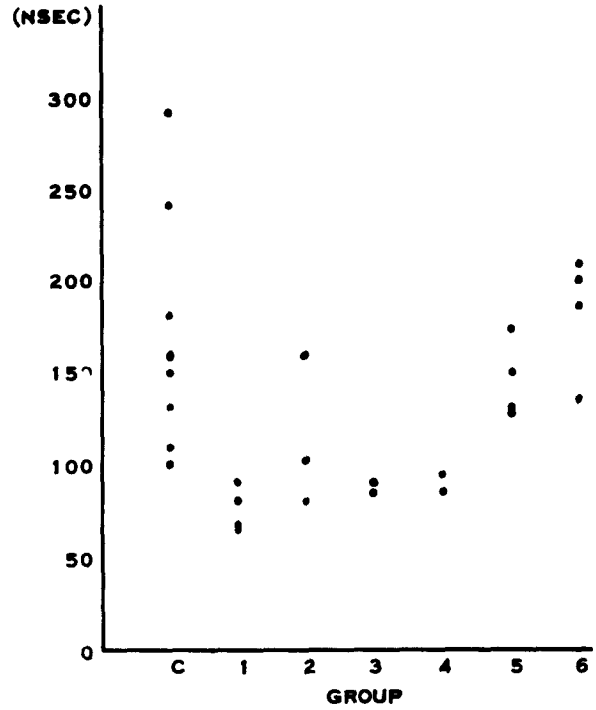
Delay Times (T_d)
Figure 10



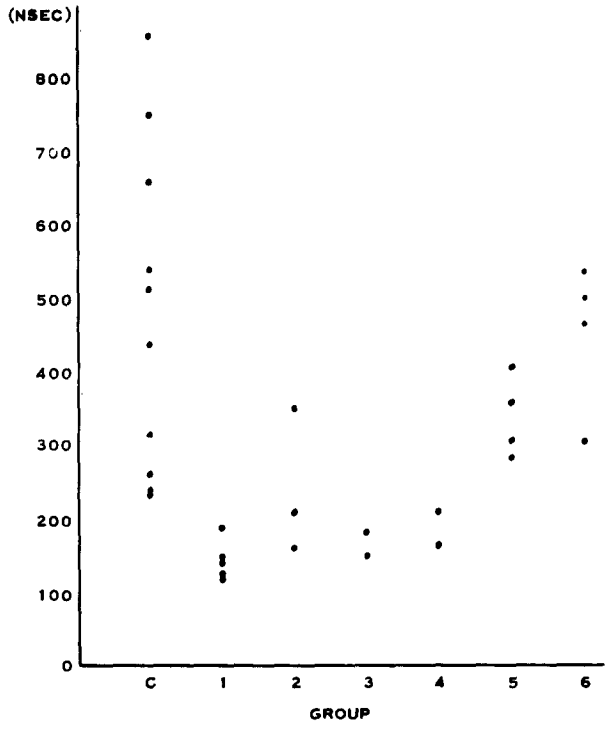
Rise Times (T_r)
Figure 11



Storage Times (T_s)
Figure 12



Fall Time (T_f)
Figure 13



Total Switching Times (T_t)
Figure 14

2.3.5.3 Use of Gold for Isolation

Gold in silicon in concentrations greater than the carrier concentration increases resistivity to near intrinsic values.[10] Two tests were run to investigate the use of this technique. In the first test, X-347 field-effect devices were used. By increasing the substrate resistivity, a high resistance is effectively put in series with the punch-through voltage, thereby decreasing the effect of any "spikes" in the gate diffusion. About 7×10^{15} atoms of gold per cm^3 were introduced by diffusion. A test slice showed that the substrate resistivity was changed to 10^5 ohm-cm, while the sheet resistivity of the diffused channel was not changed.

Table 10 compares devices on a gold-diffused slice with those on a slice which is identical except for the gold diffusion.

[10] Boltaks, B.I., Kulikov, G.D., and Malkovich, R. Sh., The Effect of Gold on the Electrical Properties of Silicon, Soviet Physics–Solid State, 2, pp. 167-175.

Table 9. Switching Times

Unit	BV_{CEO} at 10 μa (volts)	BV_{CBO} at 5 μa (volts)	BV_{EBO} at 5 μa (volts)	I_{CEO} at 20 V (μa)	I_{CBO} at 5 V (μa)	I_{EBO} at 5 V (μa)	h_{FE} at I_C = 5 ma V_{CE}= 1V	V_{CE} (sat) at I_C = 5 ma O.D. = 4.0	R_{CS} (ohms)	V_{BE} at I_C= 5 ma O.D. = 4.0	T_d at I_C = 5 ma O.D. = 4.0 (nsec)	T_r at I_C = 5 ma O.D. = 4.0 (nsec)	T_s at I_C = 5 ma O.D. = 4.0 (nsec)	T_f at I_C = 5 ma O.D. = 4.0 (nsec)	T_t at I_C = 5 ma O.D. = 4.0 (nsec)
Control Group															
1	30	72	8.4	<0.1	<0.1	<0.1	161	0.27	54	0.66	78	200	290	290	858
2	19	34	8.7	6.0	<0.1	<0.1	54.0	0.20	40	0.67	22	71	210	130	433
3	18	33	8.3	9.2	<0.1	<0.1	128	0.23	46	0.66	58	160	290	240	748
4	36	58	6.9	1.1	<0.1	<0.1	41.7	0.21	42	0.68	16	54	60	110	240
5	36	78	8.5	<0.1	<0.1	<0.1	74.0	0.21	42	0.67	31	92	260	160	543
6	35	79	8.1	<0.1	<0.1	<0.1	86.0	0.18	36	0.67	38	109	330	180	657
7	42	60	8.5	<0.1	<0.1	<0.1	22.7	0.18	36	0.69	7*	33*	120*	100*	260*
8	28	28	5.8	<0.1	<0.1	0.44	23.8	0.17	34	0.69	8*	35*	160*	110*	313*
9	16	27	7.6	40	<0.1	<0.1	31.2	0.22	44	0.68	9	43	85	100	237
10	38	80	8.4	<0.1	<0.1	<0.1	55.5	0.18	36	0.67	22	70	270	150	512
Group No. 1															
1	51	80	8.1	<0.1	<0.1	0.1	37.3	0.37	74	0.68	11	52	7	81	151
2	15.4	23	6.3	53	0.1	<0.1	27.6	0.43	86	0.68	10	39	6	67	122
3	17.5	17	8.0	—	420	<0.1	51.0	0.30	60	0.66	18	70	10	90	188
4	9.4	8.9	8.2	—	—	<0.1	28.3	0.43	86	0.68	10	40	6	69	125
5	36	51	8.0	<0.1	<0.1	<0.1	30.3	0.32	64	0.68	8	47	11	81	147
Group No. 2															
1	11.3	13.4	8.6	—	710	<0.1	40.0	0.32	64	0.68	13	55	11	81	160
2	43	88	8.2	<0.1	<0.1	<0.1	104	0.35	70	0.66	42	128	22	158	350
3	9.0	8.6	8.2	—	—	<0.1	53.8	0.29	58	0.67	21	71	13	102	207
Group No. 3															
1	7.7	7.4	8.2	—	640	<0.1	48.6	0.52	104	0.67	18	64	11	90	183
2	11.4	10.9	8.4	—	—	<0.1	34.5	0.31	62	0.68	10	48	10	83	151
Group No. 4															
1	14.9	14.4	7.8	—	—	<0.1	59.5	0.31	62	0.67	23	77	15	95	210
2	49	85	8.3	<0.1	<0.1	<0.1	42.0	0.32	64	0.68	12	54	12	86	164
Group No. 5															
1	13.4	23	6.9	77	<0.1	<0.1	114	0.66	132	0.66	48	146	16	148	358
2	7.9	8.8	8.3	—	—	<0.1	96.1	0.58	116	0.66	40	121	16	129	306
3	8.2	7.7	8.4	—	—	<0.1	76.9	0.42	84	0.65	34	104	18	127	283
4	5.3	6.8	7.1	—	—	<0.1	122	0.41	82	0.65	54	160	17	174	405
Group No. 6															
1	23	31	8.4	<0.1	<0.1	<0.1	178	0.64	128	0.66	79	210	10	200	499
2	14.5	14.0	8.2	—	—	<0.1	151	0.51	102	0.65	65	200	17	186	468
3	13.6	24	8.5	77	<0.1	<0.1	192	0.55	110	0.64	87	240	0	210	537
4	29	46	8.5	<0.1	<0.1	<0.1	89.3	0.46	92	0.66	37	118	18	136	309

Table 10. Comparisons of Devices With And Without Gold Diffusion

Unit	I_{DSS} (ma)	V_p (volts)	R_{G-G} * (ohms)
	Gold-Diffused Slice		
1	1.40	2.0	1.4×10^6
2	1.30	2.0	1.1×10^6
3	1.64	3.5	1.6×10^6
4	1.50	3.0	1.8×10^6
5	1.40	3.0	1.7×10^6
6	1.50	3.0	1.6×10^6
7	1.00	3.0	1.6×10^6
8	0.90	2.4	1.2×10^6
9	0.85	2.4	1.5×10^6
10	0.74	1.6	1.5×10^6
	Control Slice (no gold)		
1	2.40	3.0	8×10^3
2	1.10	1.6	9×10^3
3	0.80	1.2	28×10^3
4	0.95	2.0	5×10^3
5	0.95	2.4	3×10^3
6	0.88	2.4	8×10^3
7	0.75	1.6	6×10^3
8	1.16	2.4	9×10^3
9	0.90	2.0	5×10^3
10	1.00	2.0	8×10^3

*R_{G-G} = resistance from the front gate of one device to the front gates of other devices for $V > V_p$.

The second test was made on N-type slices with MPRT geometry. Isolation of N-type collector regions was achieved by gold-diffusing the slices after emitter diffusion. The quantity of gold introduced was adjusted to raise the resistivity of the N-type substrate to a near-intrinsic (100,000 ohm-cm) value while not altering the resistivity of the diffused N-type collector region.

The electrical isolation of the devices was satisfactory after the gold diffusion (about 10 megohms from collector to collector). The quantity of gold added, however, was sufficient to degrade the transistors. h_{FE} was down from about 50 in the central slice to 10 in the best of the gold-diffused slices. R_{CS} was higher for the gold-diffused samples.

The degree of isolation achieved is very encouraging. More runs will be made in an effort to increase the resistivity without degrading the devices. It is hoped that the improved ac isolation realized with the gold diffusion technique will improve the switching speed of networks.

2.4 Contacts

2.4.1 Equipment

See Section III.

2.4.2 Contact Alloying

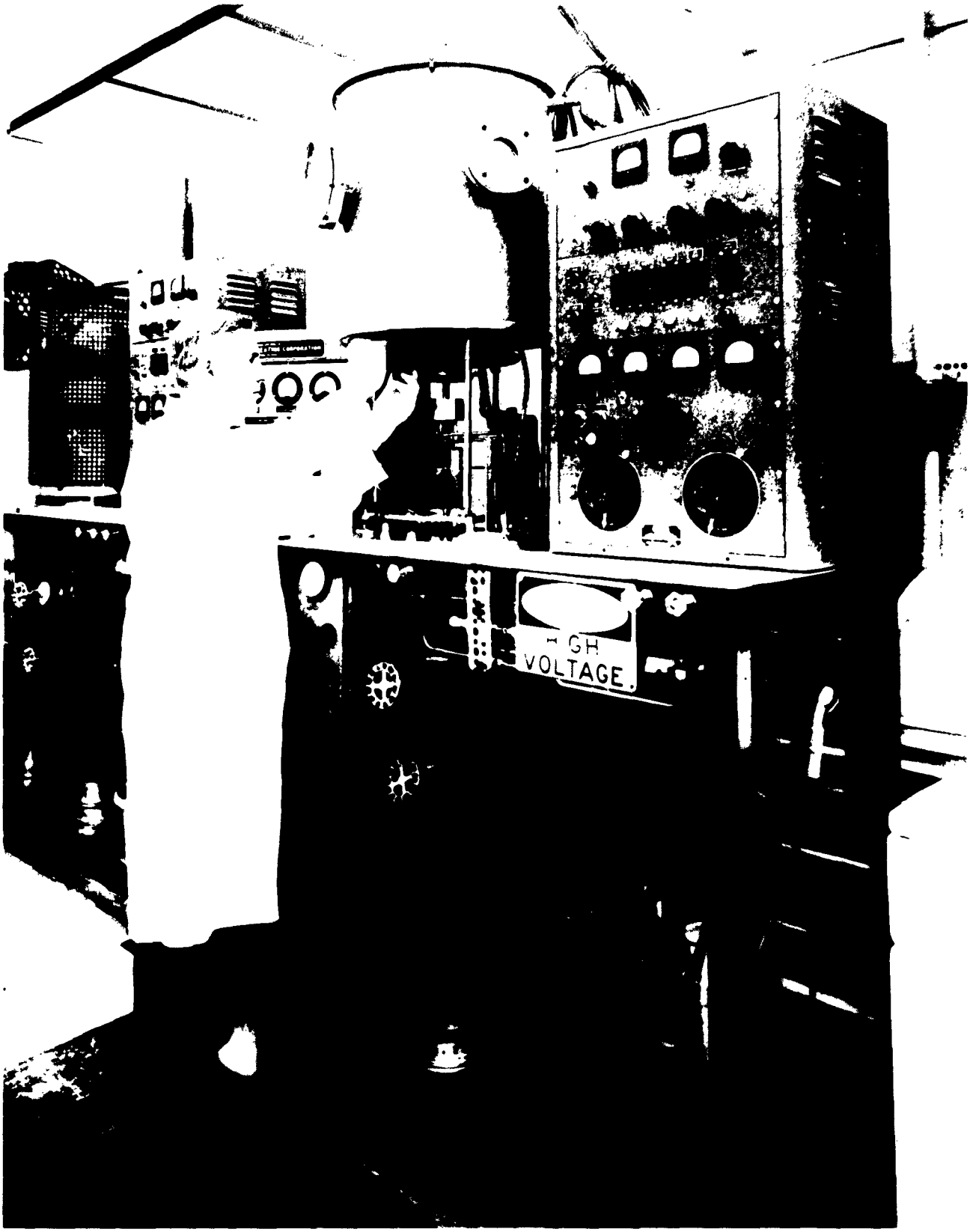
This process is working satisfactorily.

2.4.3 Contact Deposition

The ultrahigh-vacuum ion-pumped system described in the last quarterly report has been found unsatisfactory due to the large amount of helium in the ambient laboratory atmosphere. This situation is being remedied and it is hoped that during the next report period some comparative information can be obtained on ion-pumped Vs. oil-pumped systems.

Present design calls for all top contact devices and aluminum has been chosen as the contact material. An electron-beam evaporation system, Figure 15, has been installed and has satisfactorily evaporated numerous metals and nonmetals. Tests will be run comparing aluminum contacts and leads evaporated by this technique with those from a conventional, filament-type system.

In an effort to lower the resistance of the evaporated leads and to make them mechanically stronger, a program was initiated to plate a second metal onto the evaporated aluminum before the selective etching step. A reverse pattern of the selective aluminum removal pattern was obtained and the photoresist pattern which was produced defined the areas which were to be plated. After plating, the resist was to be removed and the aluminum etched using the plated metal as the "resist" over the leads.



Electron-Beam Evaporation System
Figure 15

Thus far, nickel and silver have been tried as the plated metal. Electroless nickel solution, being moderately alkaline and hot, would dissolve the aluminum film before plating began. Several solutions of electro-nickel have been tried with little success. Usually, the nickel was nonadherent, not evenly plated, and had a resistance of approximately 10 ohms/square. The poor adherence and uneven plating probably was due to the oxide film on the aluminum. In some instances, a dilute zincating strike solution was used prior to nickel plating, but the alkaline zincating solution would etch the aluminum too rapidly to be of any use.

Silver plating has been the most successful technique to date. Here again, the oxide on the aluminum has been a problem, although not as serious in this instance. Reversing the polarity for a few seconds prior to plating tended to blow the aluminum film off. The plated silver has not been very uniform, but the major difficulty has been with adherence during the subsequent etching. In trying to etch the aluminum using the silver as a pattern, the etchant undercuts (or goes through) the silver, allowing the silver plate to fall off. On probing, the resistance of the plated silver usually was greater than 1 ohm/square. Further work must be done to find optimum plating conditions for a good film, but in view of the poor results obtained thus far, this work will not be carried out under this contract.

2.5 Active Devices

2.5.1 Mounting

Since the devices being considered are top-contact devices, no ohmic back contacts are required. During the investigation of various glasses under contract number AF 3β(616)-8133, it appeared that a glass mounting scheme might be applicable for fastening the bars in the package. During this report period, a technique was developed for mounting the bars using a glass frit. This process allows bonding after mounting. The units are also much easier to handle, so that both the quality and quantity are increased. The frit used is a suspension of Corning No. 95 Pyroceram in water. After all preliminary preparations are completed, the unit is fired at 450°C for 15 minutes. For good adherence, it is necessary that the back of the bar have a lapped surface.

Section III

PRELIMINARY PROCESS STUDY SUMMARY

This section is submitted to fulfill the requirements of Item 3 of this contract. Item 3 calls for a preliminary study to determine the number and type of process steps to be performed at each station of the pilot line.

3.1 General

Process investigations conducted during the first nine months of this contract have been directed toward establishing requirements and procedures for the fabrication of SOLID CIRCUIT semiconductor-network devices on a manufacturing pilot line. Several factors have influenced the scope of these investigations, as follows:

a. The basic process was changed during the study period from the mesa process to the top-contact planar process. Successful development of the top-contact planar fabrication method has brought about significant improvements in network performance, design flexibility, reliability, and manufacturing capability. Process studies were therefore directed principally toward those operations which were unique to the top-contact planar process.

b. Process development work was performed primarily in those areas where no satisfactory procedure existed, and did not encompass all aspects of processing. Thus, development work was conducted on diffusion and evaporated-lead operations but not on the photoresist operations.

c. Process investigations were conducted with the contract objective in mind of demonstrating the capability of producing 500 good network devices per day on a pilot production line.

3.2 Top-Contact Planar Device

A discussion of a manufacturing process should start with a description of the end product which the process is designed to produce. The top-contact planar device is a semiconductor network consisting of transistors, diodes, resistors and capacitors, all formed by solid-state diffusion into the top surface of a single piece of silicon. The dimensions and positioning of the various diffused regions are accurately determined by photolithographic processing of successive silicon dioxide coatings deposited on the wafer. Evaporated metal leads are formed on the silicon dioxide insulating layer and serve to interconnect the diffused circuit elements on the surface of the semiconductor network. Assembly

is completed by thermocompression ball-bonding wires to the header, and hermetic sealing. The network element is enclosed in a glass-to-metal hermetically sealed package.

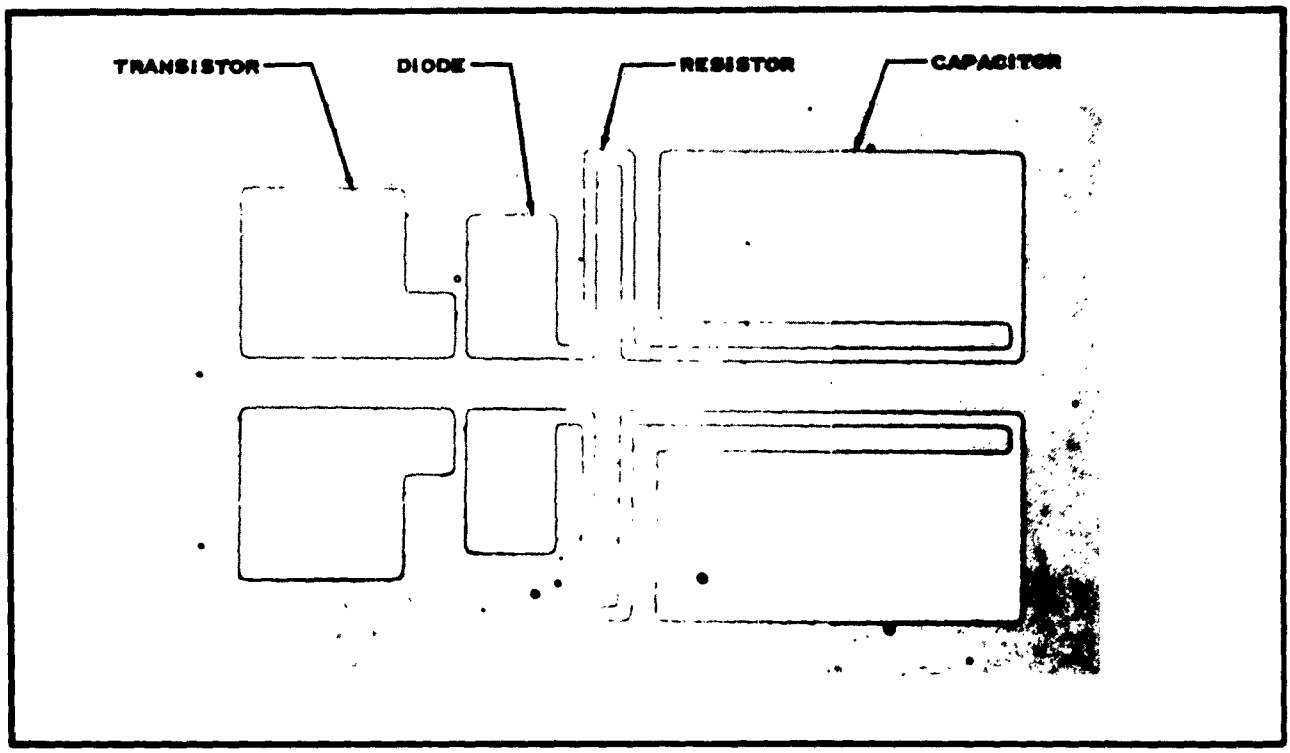
The formation of the diffused circuit elements is illustrated in the photomicrographs of Figures 16, 17, 18, and 19, and in the cross-sections of Figure 20. A complete process flow chart and description are presented in the next section of this report.

Starting with a polished silicon slice of high-resistivity, P-type material, the first step is to diffuse N-type regions to serve as NPN transistor collectors, diode cathodes, capacitor lower plates and resistor elements. Figure 16 shows a typical slice after the first N-diffusion. The resistance paths may terminate as shown at a diode and capacitor element to provide internal connections for typical logic circuit configurations.

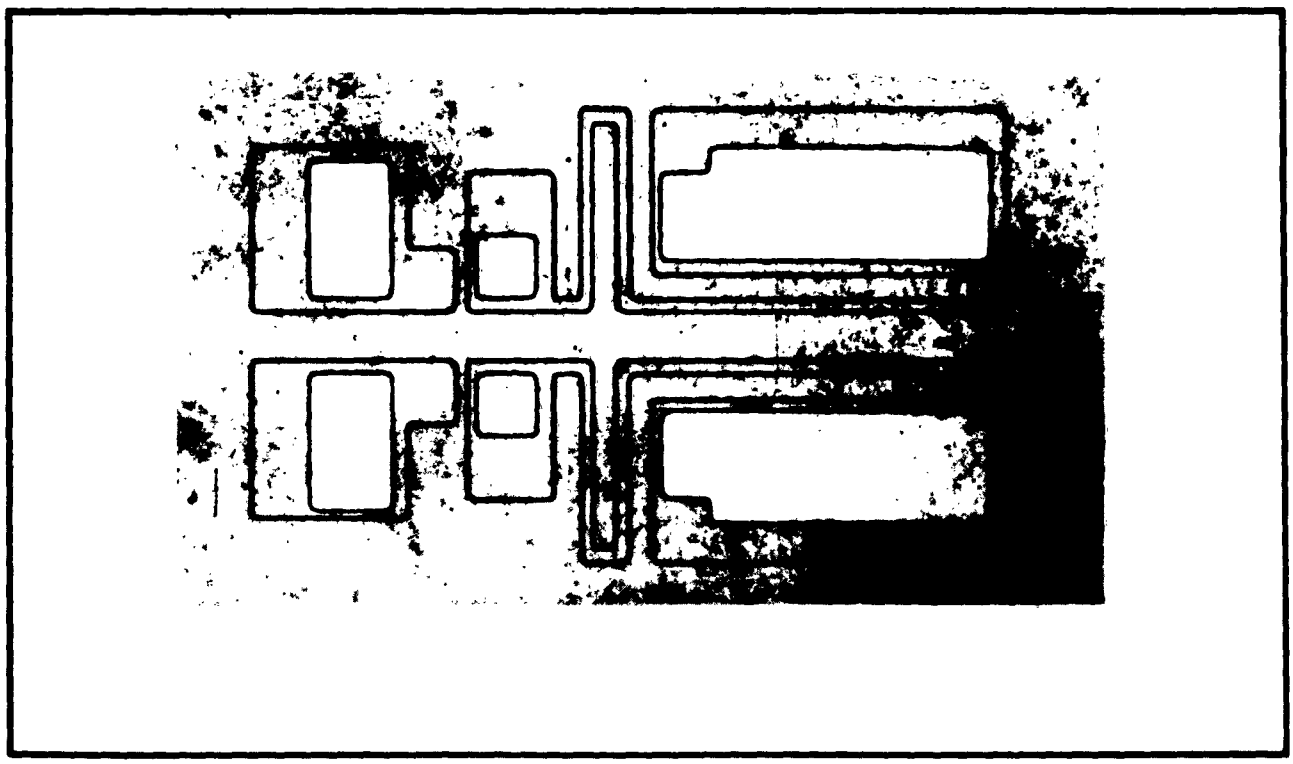
The next operation is the diffusion of P-type areas for the bases of transistors, the anodes of diodes, and the middle plates of capacitors, as shown in Figure 17. This is followed by a second, higher-impurity-concentration, N-type diffusion to form transistor emitters, the upper plates of capacitors, and low-resistance regions where contacts will be made to the first N-diffusion. Figure 18 shows the completed diffused slice.

Contact areas are formed by selective vacuum deposition of aluminum through holes in the oxide film. The contacts also overlap the capacitor elements to connect the top and bottom plates and create a three-plate capacitor with rectifying junctions. These aluminum regions are alloyed into the silicon surface to obtain low-resistance ohmic contacts, as shown in Figure 19. Point-to-point connections are then made on the insulating silicon dioxide surface by vacuum evaporation and selective removal of aluminum. The completed network is mounted in a package and terminal connections are wire-bonded to complete the assembly.

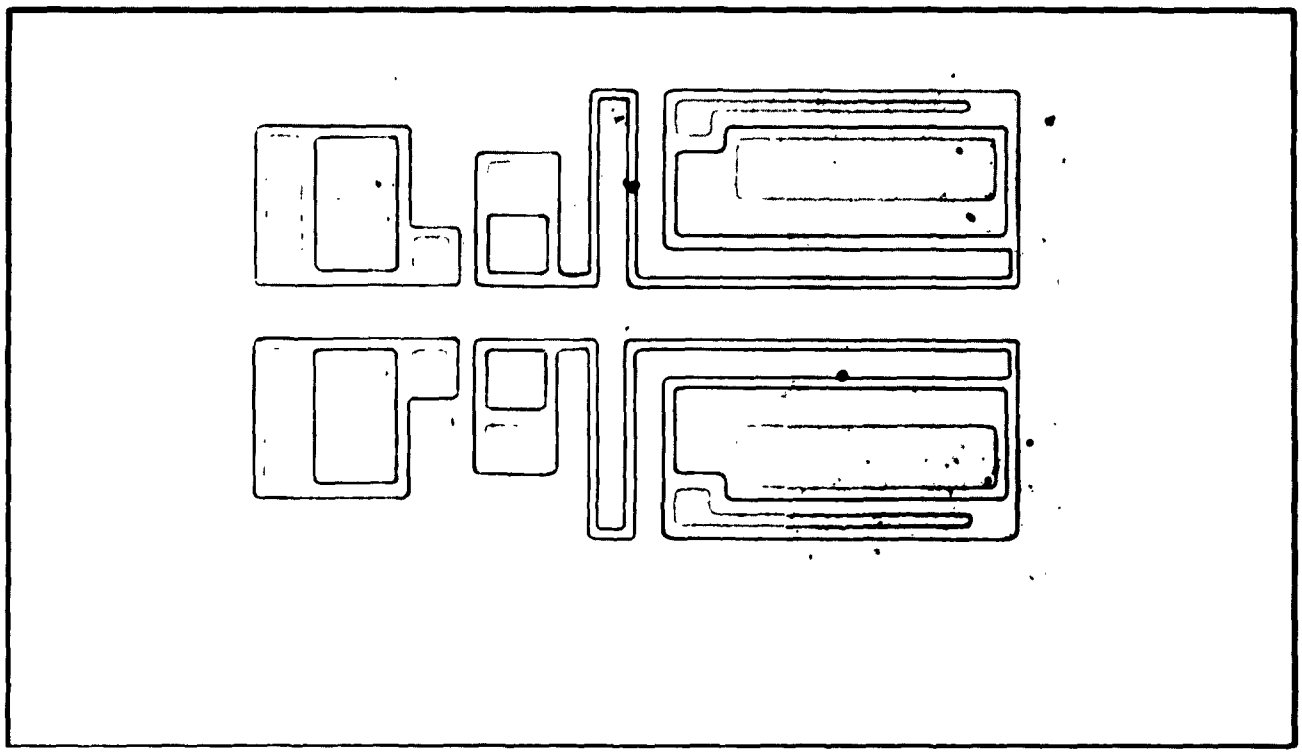
Figure 21 shows a completed top-contact planar network before sealing. The design includes six sets of similar transistor, diode, capacitor, and cross-coupling-resistor combinations, plus three sets of dual-load resistors and two large coupling capacitors. This group of components was chosen for adaptability to all typical circuit configurations required in RCTL applications. The connection shown is for a J-K flip-flop or counter network, but other evaporated lead patterns permit interconnection of the diffused planar components as a NOR/NAND network with six inputs or two NOR/NAND units with three inputs each or as in exclusive-OR network. Emitter-follower output devices may also be included for increased fan-out requirements. Figure 21 also shows the equivalent circuit representation of the flip-flop semiconductor-network device.



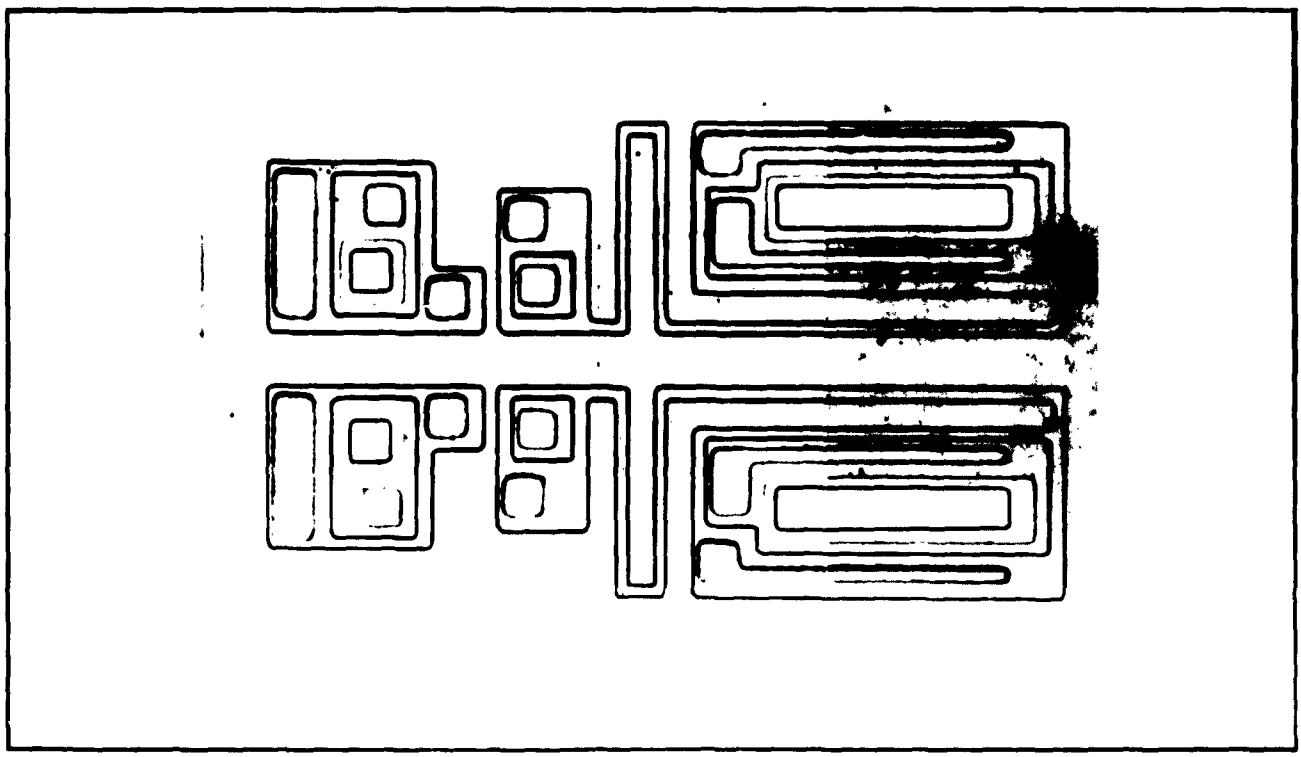
Silicon Slice After N-Type First Diffusion
Figure 16



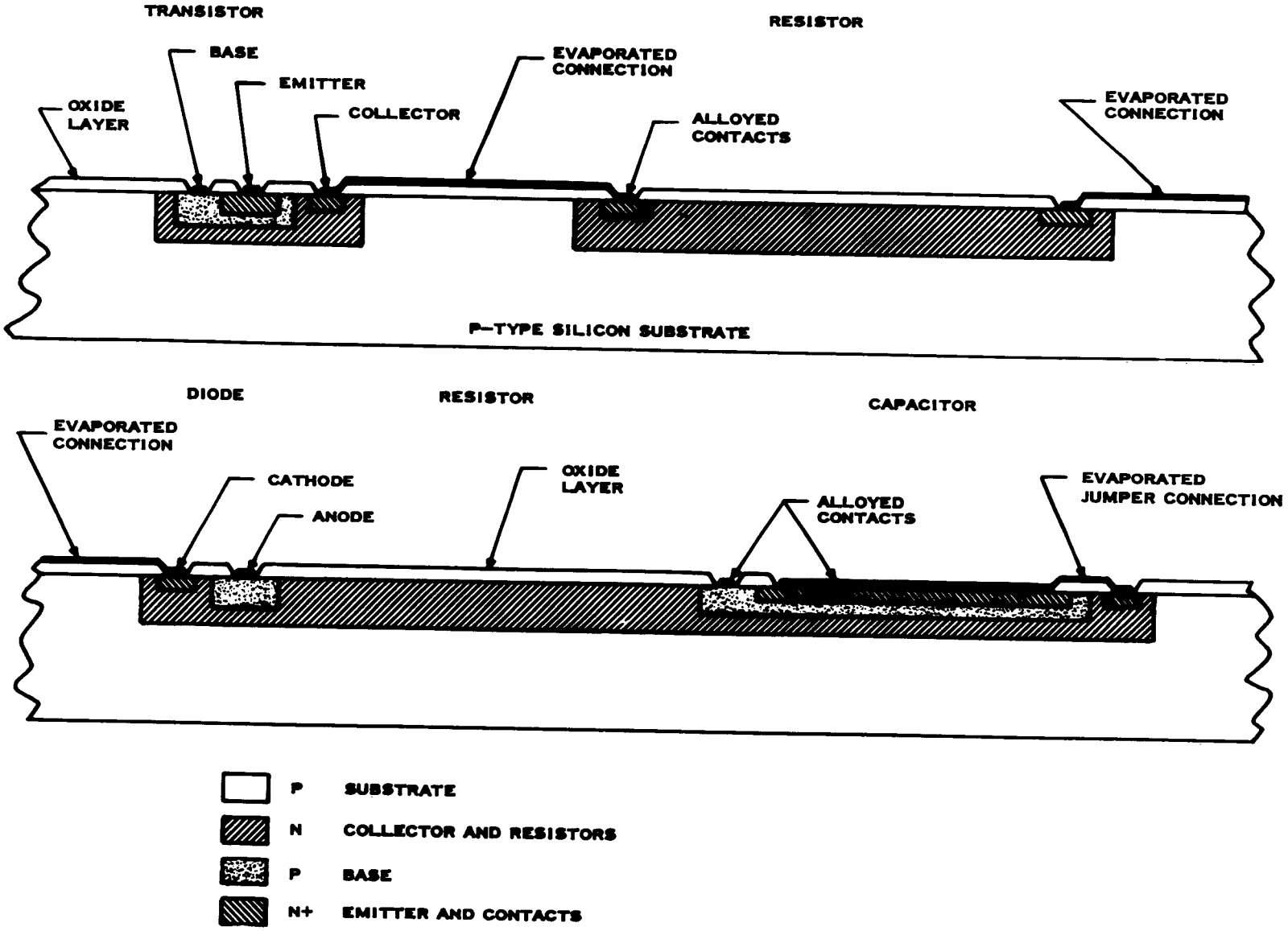
Silicon Slice After P-Type Second Diffusion
Figure 17



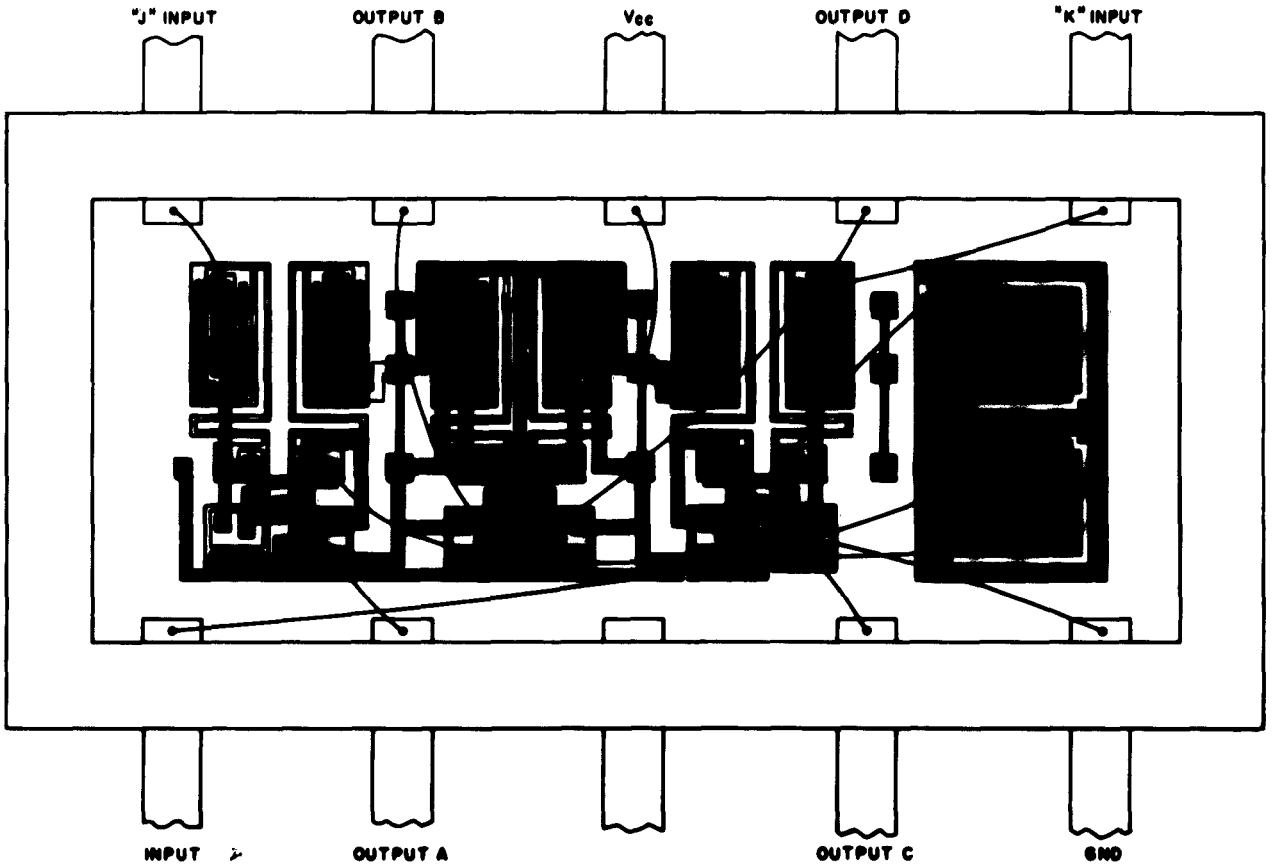
Silicon Slice After N-Type Third Diffusion
Figure 18

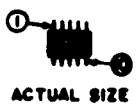


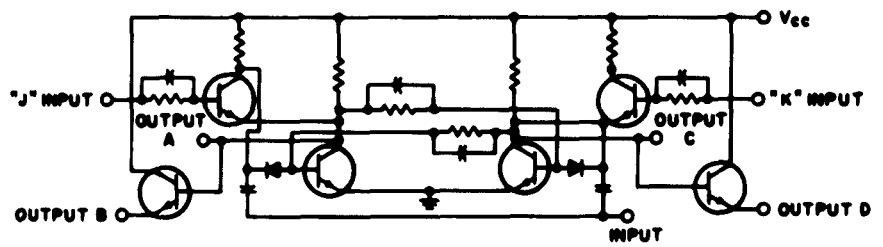
Silicon Slice with Alloyed Contacts
Figure 19



Cross Sections of Top-Contact Planar Network
Figure 20







Top-Contact Planar Flip-Flop Network and Equivalent Schematic
Figure 21

3.3 Process Flow Charts

The process flow charts for the top-contact planar network device are shown in Figures 22, 23, and 24. The first chart, Figure 22, presents the basic operations and the processing sequence while the silicon material is in round slice form. Figure 23 shows the operations and the flow of material through the process after separation of the slices into individual circuit bars. The final chart, Figure 24, details the package manufacturing operations.

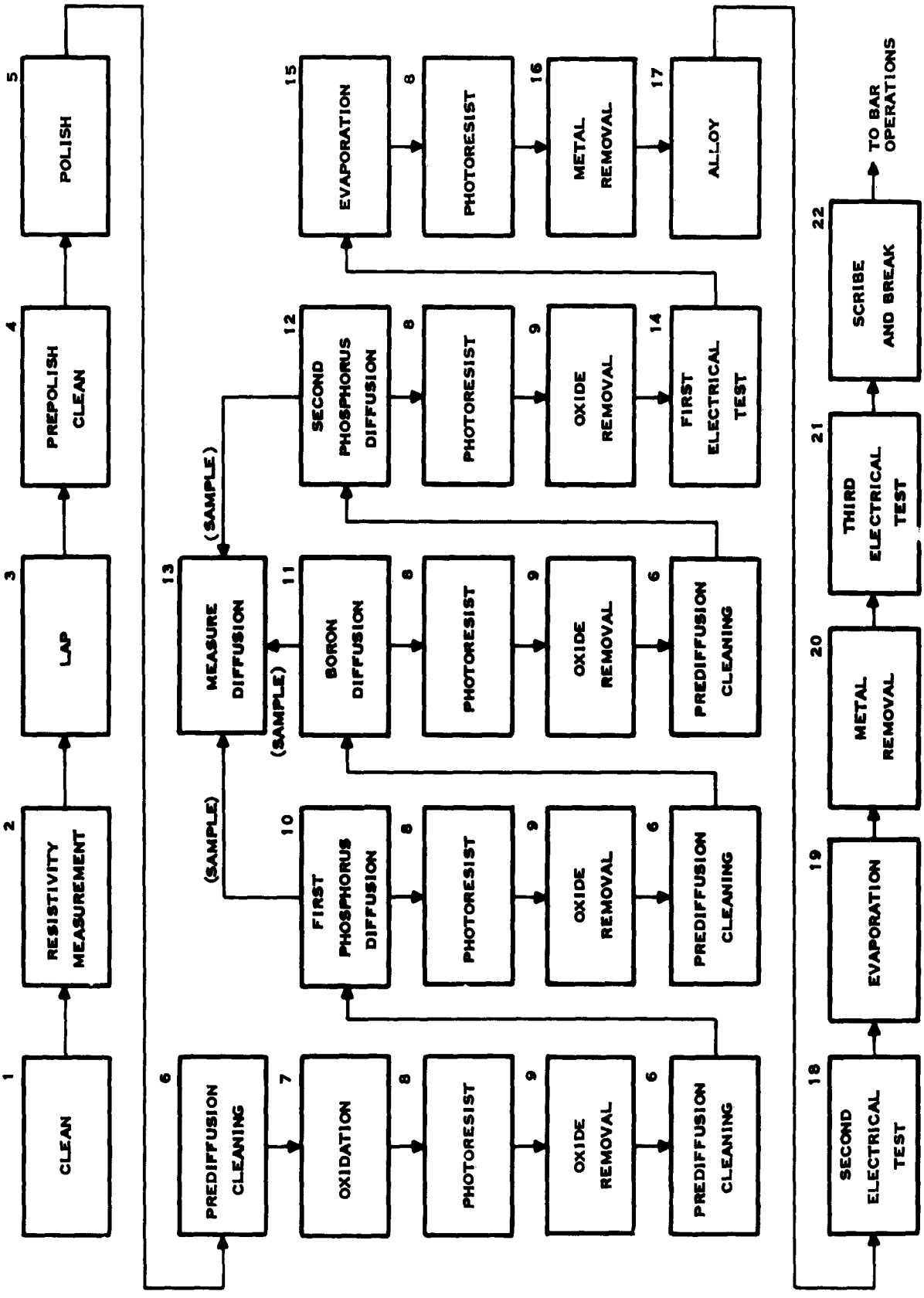
3.4 Process Description

The top-contact planar process is described in Table 11. The operations are numbered to correspond with the flow charts. The package manufacturing process is similarly described in Table 12.

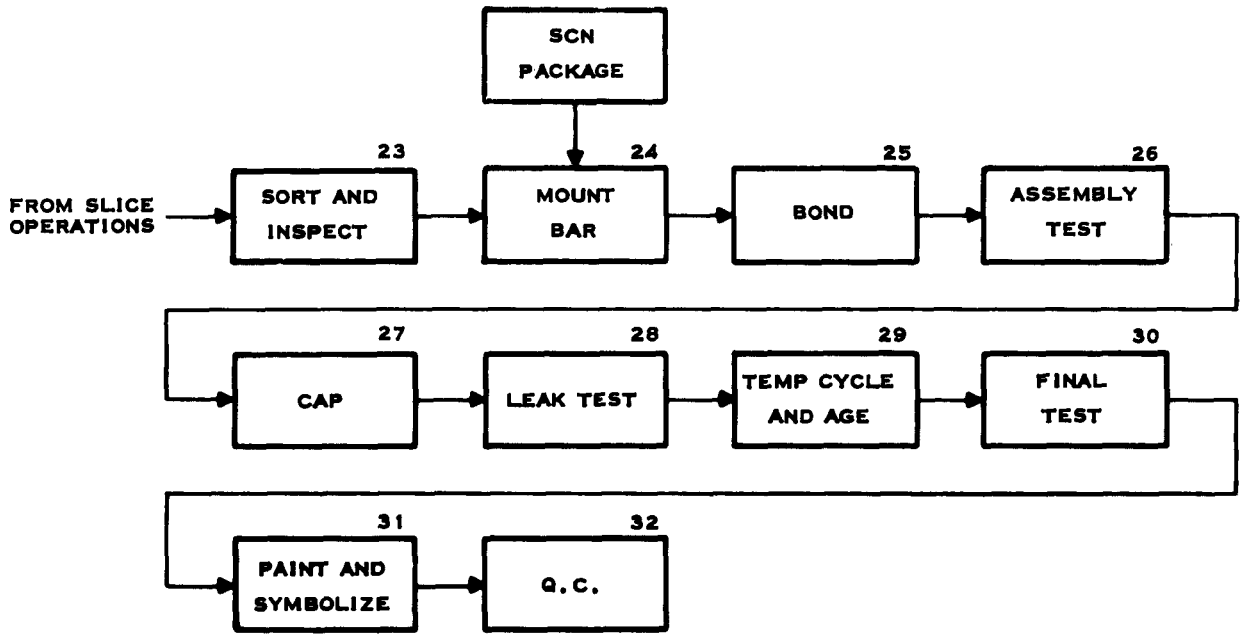
This process description is intended to aid in establishing the requirements for the design and construction of fabrication equipments to be installed and operated as a pilot production line.

Table 11. Top-Contact Planar Process Description

	Operation	Process Description
1.	Clean (Pr Resisivity Check)	Clean to remove any surface contamination that might give a false resistivity reading.
2.	Resistivity Measurement	Measure the resistivity of slices with a five-point probe and sort into resistivity ranges to help ensure better diffusion control.
3.	Lap	Lap slices on Dallons lapping machine to ensure a flat surface, remove saw damage, and obtain proper thickness for chemical polishing.
4.	Clean (Pre-Polish)	Clean slices to remove any surface contamination that might prevent obtaining a top quality polish.
5.	Polish	Chemically polish the slices in etch-polish machine to obtain a smooth surface for diffusion.
6.	Clean (Pre-Diffusion)	Chemically clean the slices to remove all surface contamination prior to oxidation and prior to each diffusion.



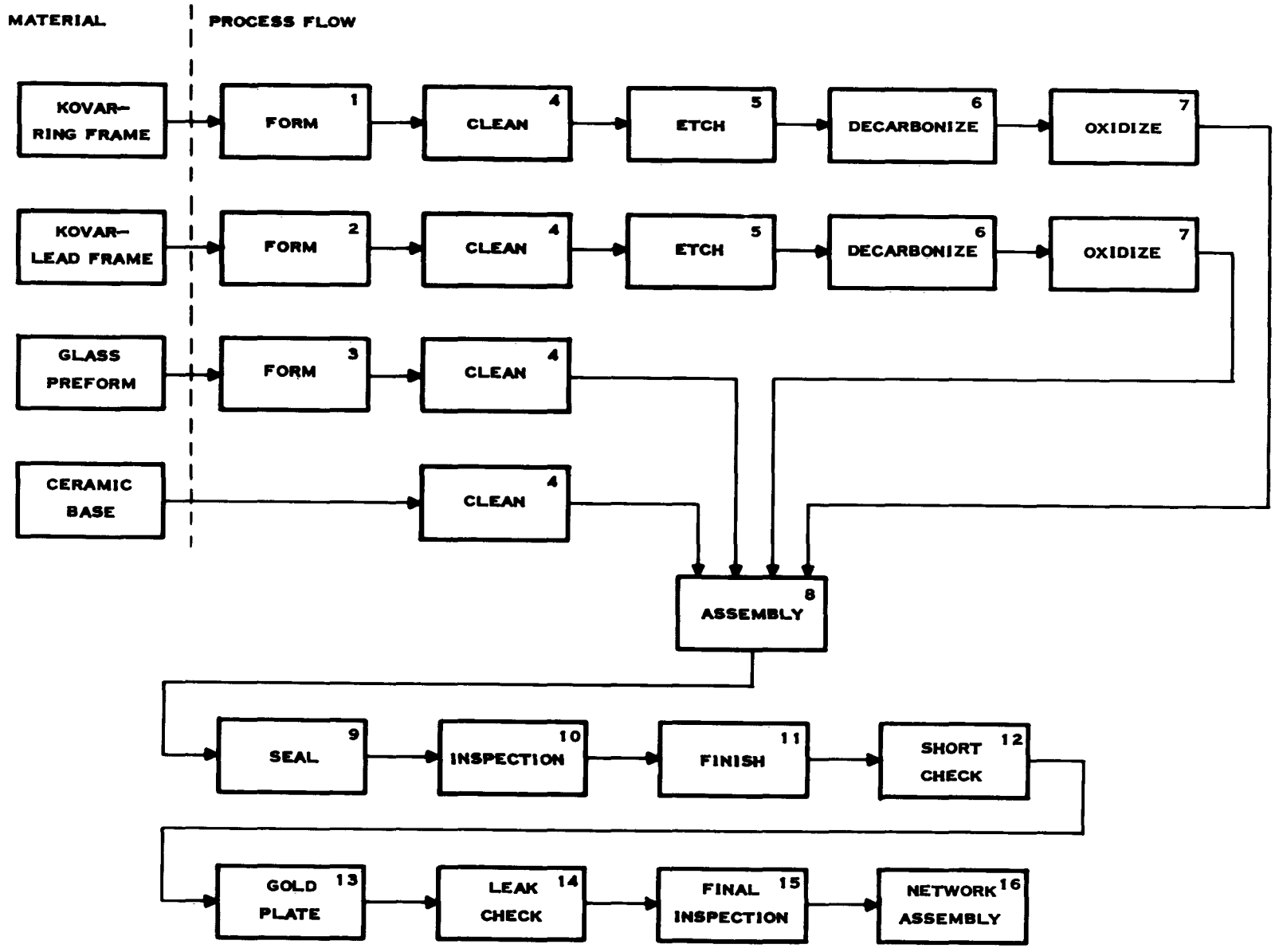
Flow Diagram of Slice Operations
Figure 22



Flow Diagram of Bar Operations
Figure 23

Table 11. Top-Contact Planar Process Description (Continued)

	Operation	Process Description
7.	Oxidation	Place slices in Hevi-Duty furnace and grow oxide layer to form diffusion mask.
8.	Photoresist	Apply photoresist film by spin-coating.
		Bake film to dry thoroughly.
		Align optical mask to register with previous pattern.
		Expose photoresist film with ultra-violet light source.
		Develop pattern by spraying solvent to remove unexposed portions of resist.
		Bake film to harden.
9.	Oxide Removal	Remove oxide layer by acid etch through photoresist pattern.



Flow Diagram of Package Manufacturing Operations
Figure 24

Table 11. Top-Contact Planar Process Description (Continued)

	Operation	Process Description
10.	First Phosphorus Diffusion	Using phosphorus in a Hevi-Duty furnace, diffuse N-regions where required into silicon surfaces not masked by oxide pattern.
11.	Boron Diffusion	Use boron in a Hevi-Duty furnace to diffuse P-regions where required into silicon surfaces not masked by oxide pattern.
12.	Second Phosphorus Diffusion	Using P_2O_5 in a Hevi-Duty furnace, diffuse N-regions where required into silicon surfaces not masked by oxide pattern.
13.	Measure Diffusion	Determine the depth of the boron and phosphorus diffusions by making optical interferometric measurements on sample angle-lapped slices. Measure surface resistivity.
14.	First Electrical Test	Electrically test sample resistor and transistor elements to reject unacceptable lots and control diffusion parameters.
15.	Evaporation	Vacuum-deposit aluminum over complete slice for contact formation.
16.	Metal Removal	Etch to remove the undesired aluminum from areas not protected by photoresist pattern.
17.	Alloy	Alloy evaporated aluminum areas into the silicon slice to form ohmic contacts for connection of leads.
18.	Second Electrical Test	Electrically test network elements with probes to select acceptable slices. (Test results are used for selection of most suitable circuit interconnection pattern.)
19.	Evaporation	Vacuum-deposit aluminum on slice for contact interconnections.
20.	Metal Removal	Etch to remove the undesired metal interconnection conductor area not protected by photoresist.

Table 11. Top-Contact Planar Process Description (Continued)

	Operation	Process Description
21.	Third Electrical Test	Perform functional circuit tests by probing completed network bars. Mark reject bars to be thrown away after slices have been scribed and broken.
22.	Scribe and Break	Diamond-scribe lines and break slices into separate bars.
23.	Sort and Inspect	Visually inspect bars to reject damaged and improperly formed bars.
24.	Mount Bar	Using Corning Pyroceram Cement No. 95, mount silicon bars in package. Fire cement in furnace.
25.	Bond	Thermocompression-bond wires to make internal connections between bar elements and package leads.
26.	Assembly Test	Test for open or improperly bonded contacts and for proper circuit operation.
27.	Cap	Seal lid to package.
28.	Leak Test	Check sealed units for hermeticity by Veeco helium-leak test plus hot-liquid-immersion bubble test.
29.	Temperature-Cycle and Heat-Age	Temperature-cycle and heat-age units to provide increased stability and reliability.
30.	Final Test	Perform operational electrical test of completed network to select good units.
31.	Paint and Symbolize	Paint and stamp symbolization on acceptable units.
32.	Quality-Control Check	Perform quality-control check on all finished units to assure a quality product that meets all electrical and mechanical requirements.

Table 12. Package Manufacturing

	Operation	Process Description
1.	Form	Punch Kovar ring frames from a die.
2.	Form	Photoetch Kovar lead frames by using the Kodak Metal Etch Resist process.
3.	Form	Lap glass preforms to size on a lapping machine.
4.	Clean	Ultrasonically clean and degrease all material in hot trichloroethylene to remove any contamination left from the forming process.
5.	Etch	Etch Kovar parts with a ferric ammonium sulphate solution to form microscopic pits for mechanical linkage of the glass and Kovar.
6.	Decarbonize	Fire Kovar parts in a wet hydrogen atmosphere at elevated temperature to provide a clean surface and to remove any gases left in the metal.
7.	Oxidize	Oxidize Kovar parts in a high-temperature forced-air oven to obtain the oxide required for a glass-to-metal seal.
8.	Assemble	Assemble Kovar parts, glass preforms, and ceramic base plate in accurately machined graphite jigs.
9.	Seal	Fire the loaded jigs in a conveyor-type, high-temperature furnace to soften the glass and form a glass-to-metal seal.
10.	Inspection	Inspect the packages for defects such as holes, misalignments, etc.
11.	Finish	Finish packages by sandblasting and/or grinding excess glass away from the inside of the package and off of the leads.
12.	Short Check	Test packages for shorts between the leads and metal ring frame.
13.	Gold Plate	Gold-plate packages by the barrel plating process to provide bonding surface for the interior leads and surface protection for the exterior parts.

Table 12. Package Manufacturing (Continued)

Operation		Process Description
14.	Leak Check	Leak test packages by using the Turco dye method and its associated developer to ensure against any large leakage (greater than 1×10^{-4} cc of helium per second).
15.	Final Inspection	Give packages final inspection to ensure against defects that would (1) hinder assembly of network, (2) allow possible leaks, (3) leave an undesirable appearance.
16.	Network Assembly	Packages are ready for assembly of the semiconductor network.

3.5 Machine Capacity Recommendations

Tables 13 and 14 summarize the important operations required for top-contact planar device fabrication and give the estimated capacity at each step of the process. Operations which are performed several times are shown once in Table 13 with the number of repetitions indicated under the capacity heading. Thus, "6 x 100" for spin-coat photoresist means that the machine must be capable of handling 600 slices per day, but each of 100 slices passing through the darkroom per day must be coated six different times.

Several minor cleaning operations were eliminated from this chart because they are simple batch operations performed with manual equipment on many slices at a time at a high production rate.

Capacity estimates on machines not yet completed or proven are very conservative, to allow considerable leeway for processing requirements. Objective designs in most cases were based on material-handling capacities several times greater than required for this contract.

Electrical testing requirements are very comprehensive at first for a newly developed device, but are later simplified by use of sampling techniques and reduction of the number and complexity of tests. The capacities shown for slice, bar, and assembled-network electrical tests will therefore be increased with experience.

Table 13. Machine Capacity Recommendations For Slice Operations

Operation	Required Capacity (slices/day)	Planned Equipment	No. Reqd.	Est. Capacity (slices/day)
Resistivity measurement	134	Resistivity test set	1	500
Lap slices	132	Dallons lapping machine	2	210
Polish	130	Etch-polish machine	1	800
Clean, preoxidation	127	Hand fixture	1	500
Oxidation	125	Oxidation furnace	1	210
Spin-coat photoresist	6 x 100	Auto. triple spinner	1	6 x 210
Bake photoresist	12 x 100	Conveyor oven	2	12 x 840
Align and expose	6 x 100	Improved align and expose machine	6	6 x 210
Develop photoresist	6 x 100	Spray developer	1	6 x 420
Oxide removal	4 x 100	Oxide etch machine	1	4 x 504
Clean, prediffusion	3 x 100	Diffusion cleaning machine	1	3 x 200
First phosphorus diffusion	114	Diffusion furnace	5	120
Boron diffusion	88	Diffusion furnace	2	120
Second phosphorus diffusion	81	Diffusion furnace	1	210
Slice probe test	3 x 70	3-point production probe set	3	3 x 84
Evaporation	2 x 68	Dual evaporator and fixture	1 set	2 x 280
Metal removal	2 x 68	Aluminum etch machine	1	2 x 105
Alloy	71	Vacuum alloying machine	1	84
Scribe and Break	68	Auto. scribing machine	1	80

Table 14. Machine Capacity Recommendations For Slice Operations

Operation	Required Capacity (bars/day)	Planned Equipment	No. Reqd.	Required Capacity (bars/day)
Bar probe test	420	Multiple-probe test set	1	420
Mount bars	374	Conveyor furnace	1	600
Bond wires	358	Thermocompression bonder	8	360
Assembly test	351	Functional test set	4	400
Cap package	281	Drybox and welder	1	420
Leak test	264	Veeco helium test	1	420
Temperature cycle and age	185	Cold chamber and oven	1 set	>500
Final test	185	Final test facility	2	210
Symbolize	100	Hand stamper	1	>500
Header manufacture	374	Conveyor oven and fixture.	1	500

Section IV

PILOT-LINE PROCESS ENGINEERING

4.1 General

Activity on the pilot line during the third quarterly period continued toward three primary objectives:

a. Manufacture of Prototype Semiconductor-Network Logic Elements

The network logic elements for installation in the first semiconductor-network computer were manufactured on the pilot line and delivered to our Apparatus Division. Deliveries were made on schedule to permit completion of the computer by the required date (first week of October). The computer is described in Section VI of this report.

b. Process Engineering Investigations

Principal process engineering effort was devoted to top-contact planar network devices. The advantages of the planar over the mesa process for all future semiconductor-network designs has been adequately demonstrated. Work was directed toward introducing planar device designs into the manufacturing operations, establishing process requirements for fabrication of these devices, and improving manufacturing yields and quality.

c. Design and Construction of Fabrication Equipment

Pilot-line activity included process investigations to establish definite requirements for the design of semiautomatic assembly machines. Prove-in of the completed equipment was conducted through controlled performance tests, after which the new machine or fixture was put into operation on the pilot production line.

4.2 Photomask Alignment

4.2.1 Mask Tolerance Investigations

Studies have been made of the problem of aligning photomasks to previously exposed patterns through six successive photoresist operations. These theoretical considerations are necessary to guide design of alignment and exposure equipment.

The extremely tight tolerances that must be held during the manufacture of semiconductor-network devices vary according to the type of circuit. In high-frequency switching circuits for operation at 1 megacycle and above, the most important considerations are switching speeds of transistors and diodes, resistor tolerances, and stray capacitances.

High-speed, low-power circuits require transistors and diodes that are comparable in speed to the 2N706A transistor and the 1N916 diode. The time constant which determines the speed of a transistor is Rb'Cc. Decreasing this time constant by reducing Rb' and/or Cc will result in a higher-speed transistor. Rb' can be decreased by increasing the area of the base contact. Cc, the collector-base junction capacitance, can be decreased by reducing the base area or reducing the impurity concentration during the collector or base diffusions. Requirements relative to base contact area are therefore conflicting. For top-contact planar transistors, the collector impurity concentration cannot be decreased because of resulting increase in R_{CS}, and the base impurity concentration cannot be decreased without increasing Rb'. The best compromise between these conflicting requirements is therefore obtained by reducing the collector-base junction area and by making the base contact as close to it as possible. Both of these solutions impose tightened tolerances for area control and spacing.

Present top-contact network designs have a minimum clearance of 2 mils between contacts and a 1-mil clearance between diffusions. Reducing these clearances to 1 mil and 0.5 mil respectively will result in a decrease of approximately 50 percent in the collector-substrate and collector-base junction capacitances. The collector-substrate capacitance is a capacitor that appears directly across the collector-to-emitter terminals and thus increases the fall-time of the collector current.

The diodes in the circuit should also be as small as possible for highest speed performance.

The resistors currently employed in many networks are made during the collector diffusion. These resistors are 1 mil in width and from 15 to 60 mils in length. The resistor value is calculated from the following equation:

$$R = \frac{\rho_s L}{W}$$

where

R = resistance in ohms

ρ_s = sheet resistivity in ohms/square

L = length in mils

W = width in mils.

The sheet resistivity of the collector diffusion varies approximately ±25 percent from the specified value, and the resistor width varies ±0.1 mil.

The worst-case resistor tolerance would therefore be approximately ±35 percent. Circuit designs using 35-percent resistors instead of 10-percent or 20-percent resistors demand an increase in the power and h_{FE} requirements. A more closely controlled resistance value may be obtained by decreasing variations in both sheet resistivity and resistor width. One method of obtaining a worst-case, 20-percent resistor is to employ the base diffusion, which has a ±15-percent variation in sheet resistivity, and increase the resistor width to 2.0 mils ±0.1 mil. The ±0.1-mil variation in the resistor width may result from the combined effects of overexposure or underexposure during production of the film mask and exposure of the photoresist coating.

Accurate alignment is required between a photomask and an underlying, previously processed pattern for five successive steps in the top-contact planar process. The minimum clearance between diffused boundaries is 1 mil. This requirement dictates that all components on the 27 possible circuit bars at each of the six photomask operations must register with a maximum error of less than 1 mil. Typical line-up tolerance of patterns during oxide and aluminum removal may be ±0.20 mil; therefore, any two of the six patterns may be off as much as 0.4 mil with respect to each other.

Other cumulative errors in the process are listed below as worst-case values; that is, 0.20 mil total for an error of ±0.10 mil, etc.

0.20 mil–original artwork and exposure of film mask

0.16 mil–step and repeat mask process

0.05 mil–expansion of film mask

0.15 mil–overexposure, undercutting, and lateral diffusion

0.40 mil–line-up between patterns during oxide- and aluminum-removal steps

0.96 mil–Total cumulative error.

Other total worst-case error between any two patterns is thus 0.96 mil. Since a total error of 1 mil is permissible for current planar network designs, these tolerances are within acceptable limits, although future designs which call for 0.5-mil clearance between diffusions for improved performance will require a reduction in these errors.

It should be realized, however, that a tolerance of 0.05 mil, or 50 millionths of an inch, constitutes an error of only 0.005 percent in a typical one-inch slice, and that holding manufacturing operations to such a tolerance will be a difficult task at best.

Examination of the preceding tabulation of potential errors reveals approaches that can reduce them somewhat:

a. A ±0.1-mil variation may be obtained by overexposure or underexposure of the film during mask making, but this is subject to close control except when the critical area is in close proximity to much larger contact areas. If closer tolerances are required, allowances may be drawn into the original artwork and exposure varied accordingly, depending upon whether a positive or negative image is needed.

   Original artwork is drawn to ±3 mils at 150 X, which gives a tolerance of 1 micron or 0.04 mil at 1 X. The drafting machine is calibrated to 1 mil.

b. The step and repeat machine is calibrated to ±0.04 mil and can be accurate to this tolerance with careful use.

c. A 20-percent change in relative humidity will change film 0.28 mil per inch (1.4×10^{-5} inch/inch/percent R.H.).

   A 20-degree change in temperature will change film 0.3 mil per inch (1.5×10^{-5} inch/inch/°F).

d. Exposure, etching, and lateral diffusion affect line widths or contact areas, but do not change centerline spacings between elements.

e. Line-up between patterns may be improved by the use of alignment marks in unused areas of the mask. A build-up of tolerances will thus be eliminated if all subsequent alignments are made to the first mark.

4.2.2 Mask Alignment and Exposure

The photoresist fabrication method for planar networks requires six successive mask-alignment operations. Each of these must be held within a ±0.2-mil tolerance to the first one in order to achieve an overall total maximum error of under 1 mil when mask construction and oxide etching tolerances are considered. Certain portions of the pattern cannot be registered with the previous pattern only, but must also be registered with a pattern several steps back in the process. Therefore, production mask alignment must be performed with extreme precision to avoid cumulative errors and attendant low yields.

Glass masks have eliminated the difficulties due to dimensional changes in plastic film masks. A fundamental problem exists, however, because the high magnification of the microscope required for accurate registration limits the field of view to a very small portion of the slice.

It is therefore very time-consuming to obtain perfect alignment everywhere on a slice using a simple trial and error method with one spot at a time. Furthermore, there are mechanical problems in holding the fragile slice and mask in close proximity without touching and in providing dependable manipulators with quick traversing plus fine adjusting capabilities.

A systematic approach is planned to improve alignment techniques; it will include the following steps:

a. Four new alignment and holding jigs are under construction at present to improve the present method by use of excellent mechanical manipulators.

b. A dual-image optical system is being constructed by the Optics Department of Texas Instruments Apparatus Division to provide two widely separated observation points for simultaneous alignment of an entire slice in one operation. This will be a microscope attachment which can be used with the mechanical fixture to eliminate movement of the microscope during alignment and simplify the operation to a single step.

c. Various light sources are being evaluated to reduce exposure times in accordance with reduced alignment times. High-intensity, even, and cool illumination is required in the ultraviolet region for fastest exposure. A quartz lens has been ordered to obtain light transmission in the ultraviolet portion of the spectrum where glass is opaque. High-intensity mercury-arc, zenon-arc, and carbon-arc sources will be evaluated with and without concentrating lenses.

d. Future requirements for alignment and exposure at production levels of 500 good units or more per day will be handled by advanced systems now under investigation. One of these is a refinement incorporating all the best techniques listed above plus the important feature of prealignment of silicon slices at initial placement in the fixture. The slices all have a flat on their circumference for orientation of the proper crystal plane in scribing. This flat in conjunction with a mechanical clamping fixture will permit the operator simply to drop each slice into place to within a few thousandths of an inch of perfect registration under the microscope field, thereby reducing alignment time and removing all ambiguity or confusion from the operation.

4.3 Darkroom Elimination

A darkroom with controlled nonactinic illumination is customarily used for all photoresist operations. The flow of material according to the process flow chart is into and out of this darkroom six times. This

is acceptable for laboratory operations, but a high-level production line could be planned to operate more efficiently around a straight flow path. Accordingly, investigations were conducted to determine the feasibility of photoresist processing in the open production-line area.

A test area was set up by installing a 4-foot by 8-foot sheet of yellow plexiglass about 6 feet above the floor, over an assembly bench, to block out direct overhead room light. This arrangement represents approximately the poorest light shielding that might be used in production. Silicon slices were coated with KMER in the usual manner and allowed to rest on the bench top for varying periods of time, after which they were exposed and developed in the pilot-line darkroom. The results showed that room light exposure intervals of 10, 25, and 45 minutes caused no detectable fogging of the photoresist. A three-hour exposure caused the beginning of pattern degradation, and an overnight exposure fogged the photoresist badly.

These tests indicated that slices may be processed through photoresist steps in simple light boxes on the production line without the confinement of a darkroom. If a new, high-speed photoresist coating, now under development by Eastman Kodak, is adopted, a special darkroom, or at least more stringent light-control conditions, may become necessary again.

4.4 Electrical Probe Testing

A feasibility study was made to determine a method for making probe contact to selected active areas on a slice. These contact areas may be as small as 3 mils square with separations of as little as 2 mils. It is necessary to make contact to groups of two or three spots at a time for test-probing resistors, diodes, transistors and capacitors during the processing of slice elements. In addition, it is desirable to probe ten or more points simultaneously in order to make operational circuit tests on a completed bar element before package mounting and bonding.

An insulating plastic plate was drilled with holes located over the emitter, base, and collector contacts of a transistor element. Three-mil tungsten wires were held in alignment in these holes and individually sprung by casting a flexible silicone rubber potting compound around them. The feasibility of this probe method was proven. More complex hole patterns would probably be created by photoetching holes in Corning Photoform glass. Practical test fixtures will be designed to perform automatic indexing and alignment movements of the probe head.

4.5 Bar Scribing

Diamond scribing and breaking slices into bar elements has replaced the deep-etching separation method. Deep etching is necessary to produce

irregularly shaped silicon bar elements, but scribing techniques can be used for the uniform rectangular shapes of top-contact planar designs.

The crystal orientation of the silicon slice was found to be important in obtaining good yields on breaking. A crystal grown in the 111 direction will give slices whose surfaces are parallel or perpendicular to the 110 plane for rectangular bars. Proper orientation is obtained in crystal production by grinding a flat parallel to the 110 plane on the starting crystal. This flat also assists in maintaining slice orientation throughout the photoresist mask-alignment operations.

4.6 Contact Bonding

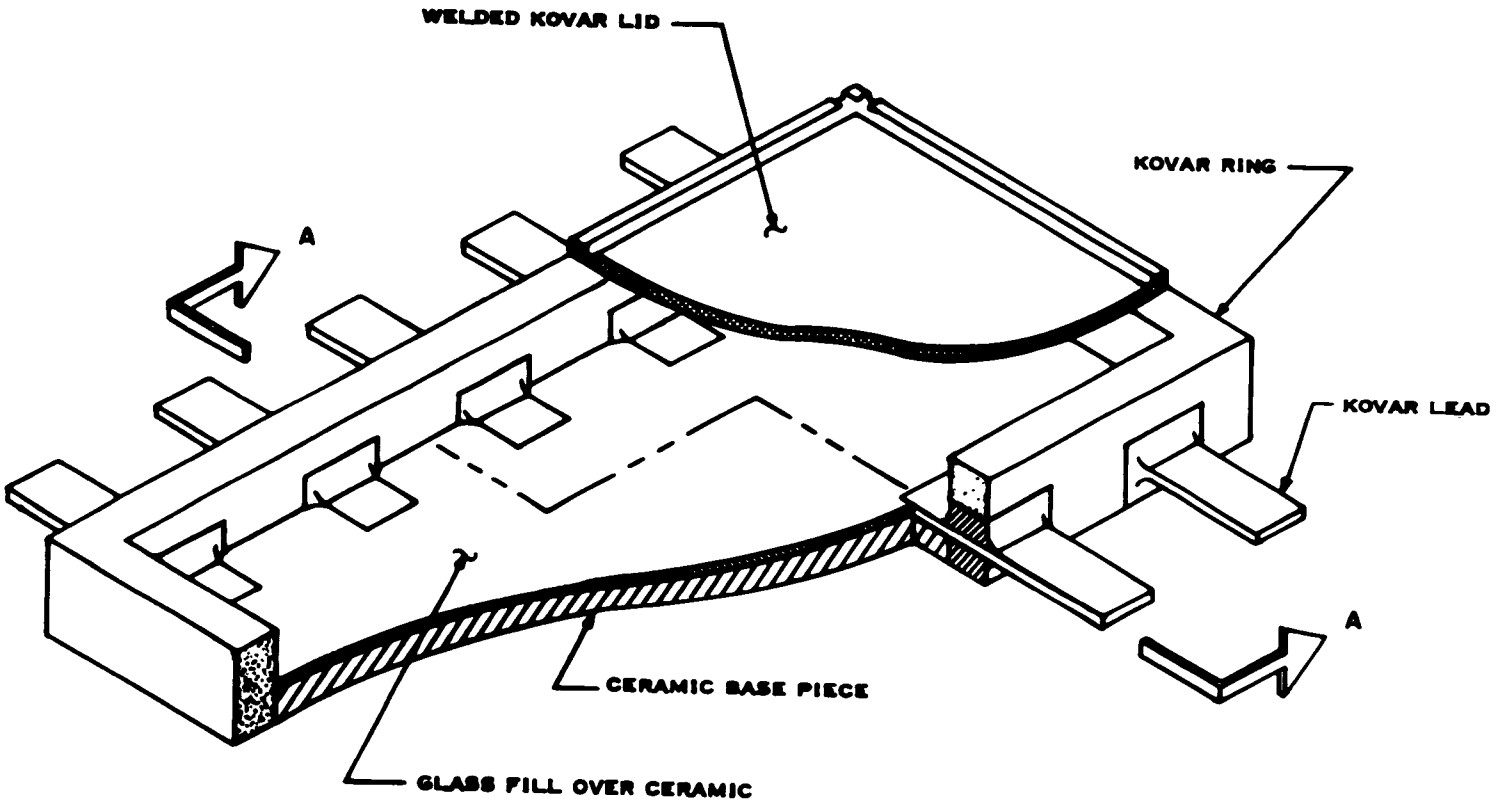
Thermocompression ball-bonding of 1-mil gold wire is employed to make contacts between the alloyed aluminum contact areas on the silicon bar and the package terminals. Ball-bonding provides a strong, reliable contact, but can be performed on only one end of the wire. Chisel-bonding has been acceptable for connecting the gold wire to the gold-plated terminals. Additional strength and reliability have been provided by bonding a second gold ball on top of the chisel bond. The loose wire is cut off close to the ball which covers and strengthens the chisel-bonded connection.

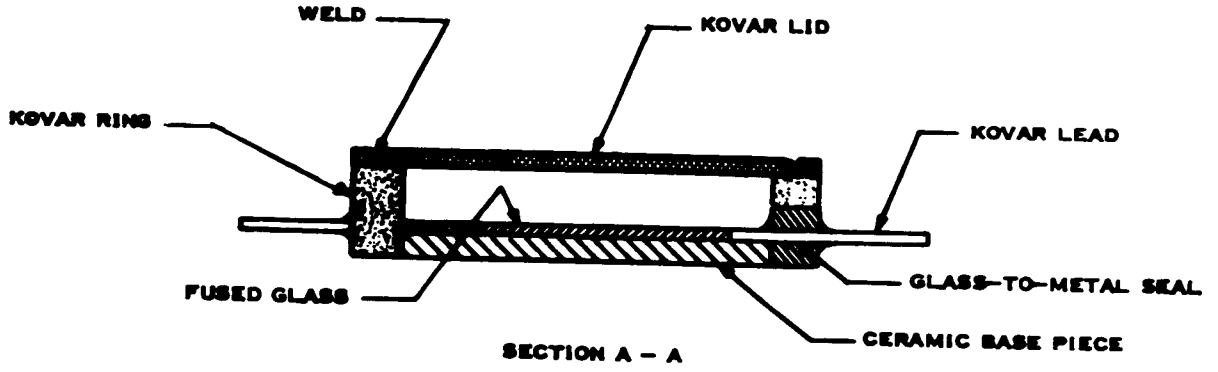
4.7 Network Packaging

Development of a hermetically-sealed package was completed by Texas Instruments prior to this program. Within the past year, the package has been modified and techniques developed to perform final sealing by welding instead of soldering. Tools have been acquired with company funds for forming package parts, and experimental lots are being produced. A welded package will be used on the pilot production line. Proving of equipment for manufacture and final sealing of the welded package is therefore a part of the Manufacturing Methods Program.

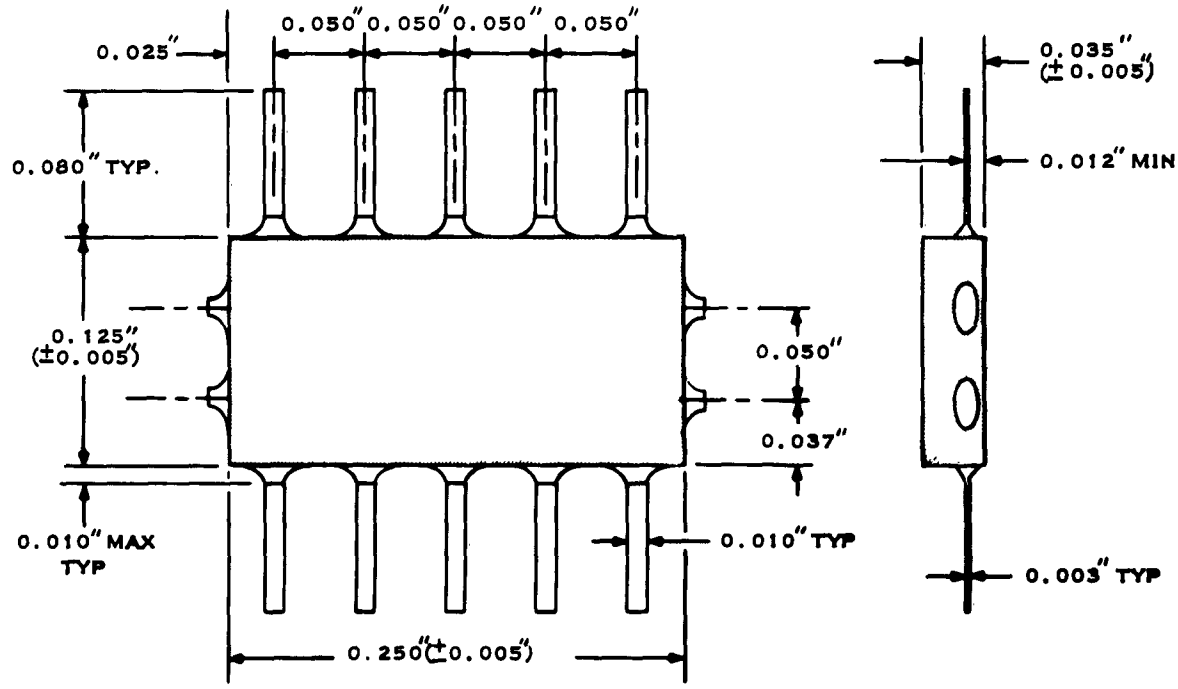
4.7.1 Package Design

The proposed welded semiconductor-network package design is shown in Figure 25. It is a hermetic enclosure which employs metal-glass-ceramic seals. The unique feature of this package is the outer frame made of Kovar. It is castellated to provide insulated feed-through tab connections and also to permit the passage of welding current through the lid and frame from top to bottom. The high-density alumina ceramic plate provides a strong bottom surface for alignment of the tab leads during assembly. The Kovar, ceramic, and hard glass are matched in expansion coefficients to provide an assembly usable within the temperature range of −65°C to over +300°C.





Welded Semiconductor Network Package
Figure 25



Semiconductor Network Package Dimensions
Figure 26

The ten terminal leads and the surrounding frame are formed from one piece by means of photoetching techniques. The glass which seals the ceramic and metal parts together starts as a flat, rectangular preform and flows outward to fill the holes in the castellations during the firing operation in graphite holding fixtures.

The outline dimensions of a completed network package are shown in Figure 26. Ten leads are normally used and are sufficient for most circuit designs. Provisions will be made on permanently tooled parts for two additional leads at each end. These four additional leads may serve as test points during device fabrication, but will be cut off after final testing. They may be employed as additional terminals if required.

4.7.2 Flow Chart

The flow chart and process description for manufacturing packages are presented in Figure 25 and Table 12 in the Preliminary Process Study section of this report.

4.7.3 Capping of Packages

The metal frame which extends from top to bottom of the package makes it possible to use several cap-sealing methods, such as spot, seam, or projection welding, thermocompression bonding, or electron-beam welding. Experience with resistance welding at Texas Instruments indicates that this method offers the greatest advantages for production sealing, but the welded area must be small and carefully controlled by a suitable projection on the lid to avoid overheating the metal castellations during welding.

Section V

PILOT-LINE EQUIPMENT

This section describes the processing equipment for the pilot production line. Machines which are completed, in construction, or in advanced design stages are discussed.

5.1 Chemical Polishing Machine (Figure 1)

Design has been started on a chemical polishing machine to carry out the principles described in Section II of this report. The most significant part of its design is the slice-holding fixture, a prototype of which is shown in the photograph. The production machine will include high-capacity water quenching and automatic timing of the complete cycle. Estimated capacity is 200 slices per hour.

5.2 Temperature Profiling Machine (Figure 27)

A machine has been constructed to automatically measure and plot the temperature profiles of the hot zones in diffusion furnaces. This must be done regularly on each furnace to maintain precise control of the diffusion processes. The machine consists of a constant-speed motor-driven traversing mechanism to move a thermocouple slowly through the furnace tube while a temperature record is plotted on a strip-chart recorder. The Leeds and Northrup recorder is a multipoint model which can be used to monitor the temperatures of all the furnaces continuously by means of auxiliary thermocouples.

5.3 Photomask Alignment Fixtures

Design work is under way on an improved slice and mask alignment fixture for photoresist exposure. This fixture consists of a modified Unitron toolmaker's microscope slide assembly with attachments for holding slices and film. Slices are held on the movable stage, which is given X, Y, and rotational movements by means of micrometer screws. The film mask is clamped in a rigid frame and is fixed in position with respect to the alignment stage. Separate modified frames will be provided for glass masks.

5.4 Photoresist Baking Ovens

Several tests have been run to evaluate the performance of the photoresist conveyor baking ovens described in the last report under this contract, ASD Interim Report 7-865 (III). Slices were coated with KMER and run through the ovens on a 10-minute cycle at temperatures ranging from 119°C to 180°C. The baking time was next varied from 12 to 20

Temperature Profiling Machine
Figure 27

minutes at 122°C. None of these combinations produced a properly baked film.

The problem was solved by blowing dry air into the oven to remove solvents given off in the baking operations. Final results were very satisfactory and the conveyor ovens are ready for use.

5.5 Photoresist Developing Machine

This machine spray-develops the exposed photoresist film by removal of the unexposed areas. It comprises a rotating wheel on which the wafers are placed to be carried under oscillating spray heads. Twelve separate sprayers permit flexible programming of sprays of developer, water, alcohol, or air. Estimated capacity is 420 slices per hour.

Construction is under way and scheduled for completion in November, 1962.

5.6 Oxide Etch Machine

This machine removes silicon oxide by etching in hydrofluoric acid. Slices are manually loaded into holding fixtures on a rotating table and automatically indexed and lowered into etching and rinsing baths. The original design is being modified to provide a more compact machine for better utilization of bench space and etchant volume. Estimated capacity is 288 slices per hour.

Design will be completed early in November 1962.

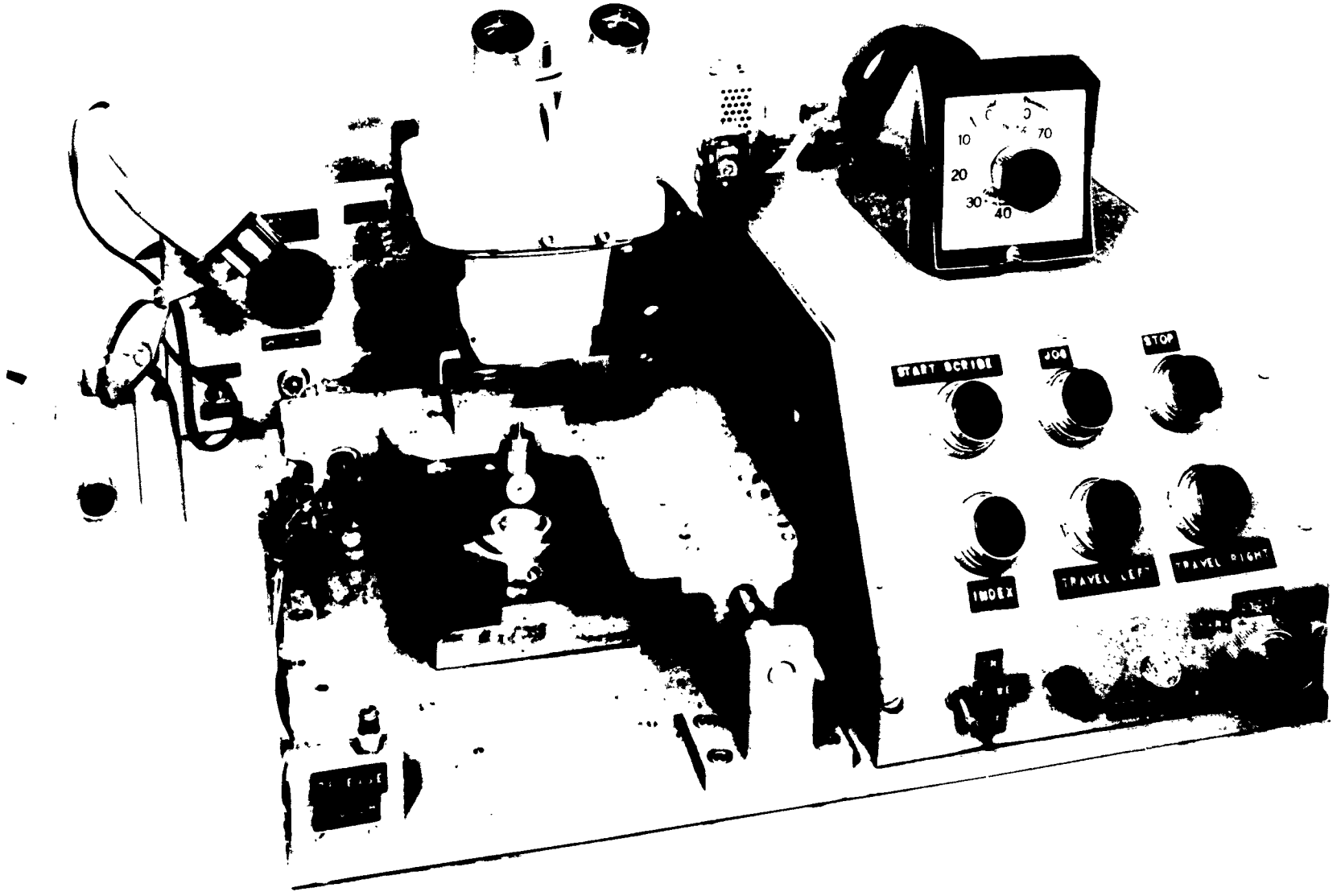
5.7 Mesa Deep-Etch Machine

This is an in-line conveyor machine to etch mesas and deep-etch slices for separation into bars. Slices are mounted on carrying blocks and indexed through etching and washing stations. Etchant is applied through a submerged spray head by means of a pump and recirculating system.

The new top-contact planar process does not require this machine, which is scheduled for completion early in October, but it will be installed for prove-in and use on special designs.

5.8 Evaporation Fixtures

Two fixtures are being constructed for vacuum metalization of silicon slices. Each consists of a pair of hemispherical domes surrounding the evaporator filaments. The fixture will hold 41 slices in the lower dome for all-over evaporation and 15 slices in the upper dome for masked evaporation. The domes are equipped with heating and cooling coils for evaporation onto a hot substrate.



Bar-Scribing Machine
Figure 28

Completion is scheduled for the end of October.

5.9 High-Vacuum Evaporator

The Kinney dual, high-vacuum evaporator, which was described in the last report, has been modified by the manufacturer to improve operation of the hydraulic bell-jar lifting mechanisms. The original design did not provide reliable operation with water pressures available at that time. The water lifts were replaced with air-hydraulic lifts, and the vertical guiding system was improved. Operation is now very satisfactory.

5.10 Vacuum Alloying Furnace

This machine alloys evaporated aluminum into the silicon by means of radiant heat and rapid cooling in a hard vacuum. The system is installed, but a ceramic heater insulator is being replaced with one of quartz to lessen out-gassing. The vacuum system is also being altered to incorporate an improved valve and pump for faster evacuation.

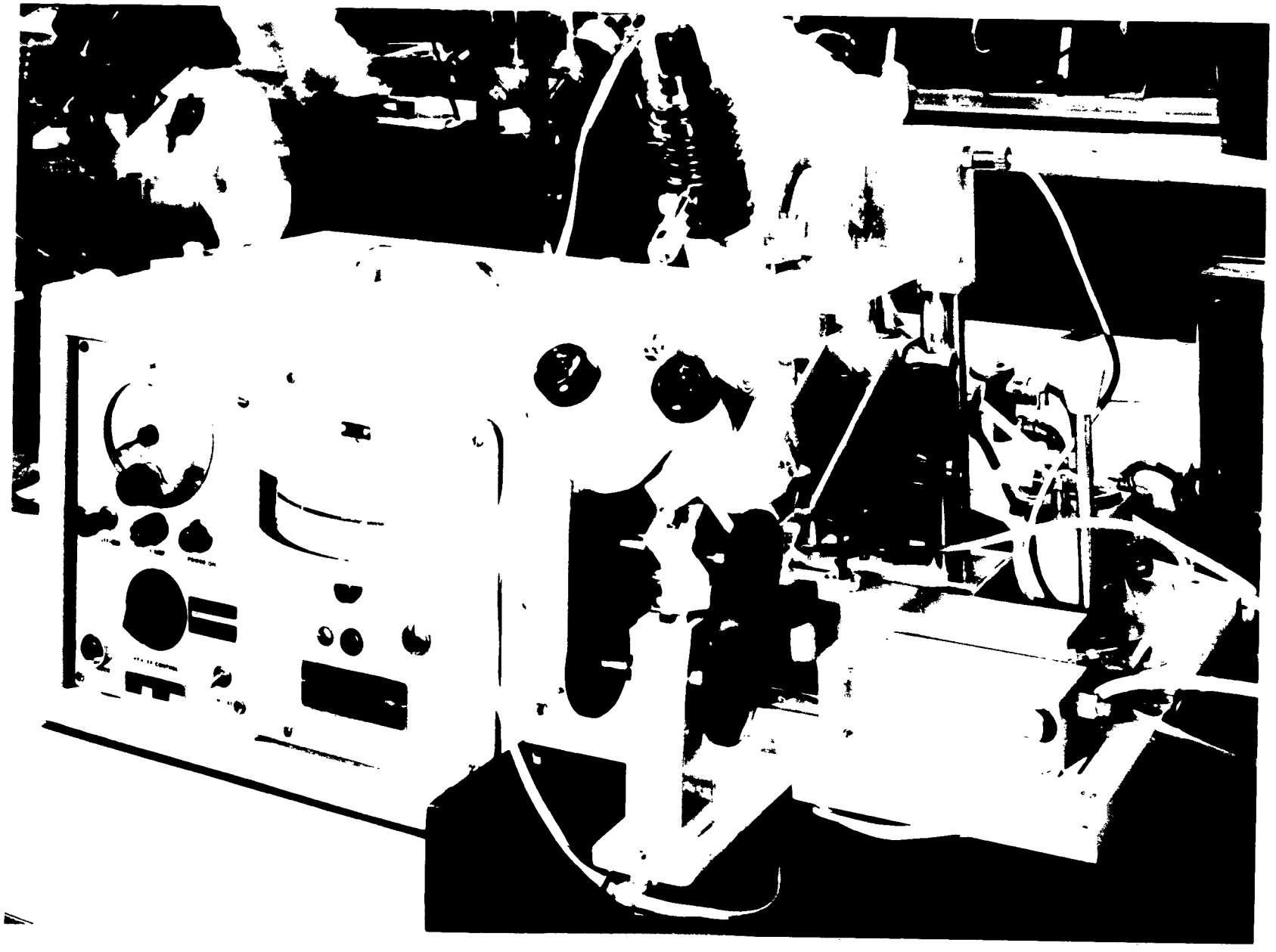
5.11 Bar-Scribing Machine (Figure 28)

This unit scribes completed slices with a diamond stylus for separation into individual bars. It replaces the slower, deep-etch process employed for top-contact planar devices. A reciprocating head carries the diamond point, which lifts at the end of each stroke and indexes automatically to the next interval. It is adjustable in 10-mil increments. Slices are held in place by freezing them to the carrier with CO_2 gas. The carrier may be rotated 90 degrees to cut rectangular bars, and initial alignment is accomplished by micrometer manipulation using reference cross-hairs in a microscope. Machine capacity is estimated as 30 slices per hour.

Electrical wiring is being completed and the machine is scheduled for operation around the middle of October. This is a prototype machine which was modified from an existing model. An improved machine will be built for pilot-line use

5.12 Electroglas Ball Bonder (Figure 29)

An Electroglas nail-head or ball-bonding machine has been purchased for evaluation in wire-bonding network connections. This machine is semiautomatic and is expected to reduce bonding time. The sequence of operations begins with the loading of a unit into a heated holder which rotates 180 degrees from the load and pre-heat position to the bond position. The bonding capillary may be moved accurately in the X and Y directions by means of a "joystick" manipulator arm which has two buttons on its handle to control the lowering of the bonding tube and



Electroglas Ball Bonder
Figure 29

balled wire. One button lowers the tube to within a few mils of the silicon to facilitate precise placement, and the second button causes the bonding capillary to drop and form the bond. After this point, the sequence is automatic. Bonding pressure is held for a timed interval, after which the capillary is raised, withdrawing wire as it moves, until a pointed flame cuts off the wire and forms a new ball on the wire in preparation for the next bond.

Some modification of the holding fixture and microscope mount will be required to adapt this machine for network assembly.

5.13 Vacuum Oven and Dry Box (Figure 30)

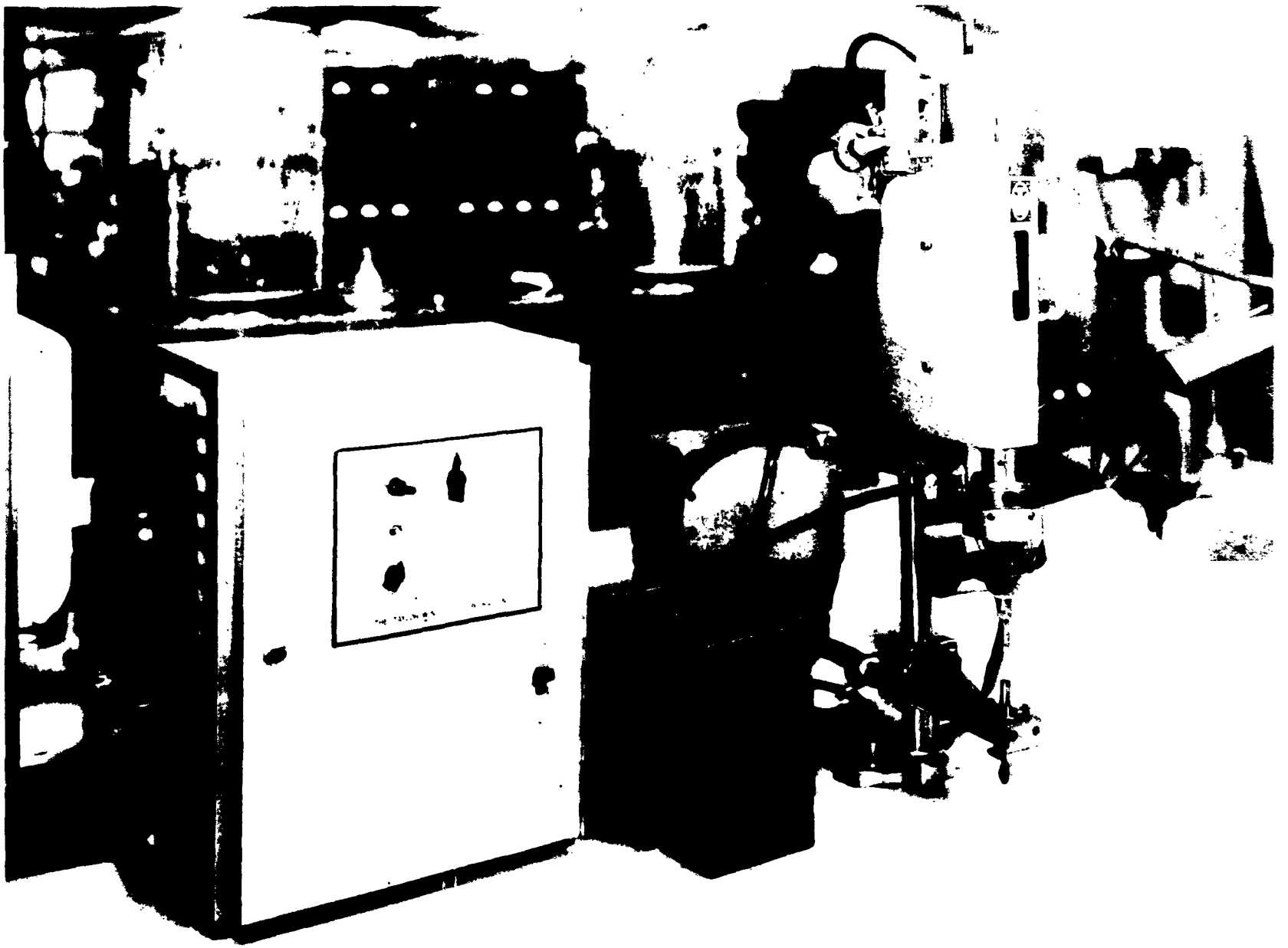
This unit consists of two hermetically sealed, 36-inch boxes with a bulkhead between them. There is an airlock on the right box and a 400°C vacuum oven on the left box. It includes a microscope mount, mechanical vacuum pump, cold trap, and automatic controls. It will be used for final baking and encapsulation in a controlled atmosphere. A welder will be installed after a suitable design is proven.

The system has been received and electrical wiring is under way. Installation is scheduled late in October.

5.14 Encapsulation Welder (Figure 31)

A Taylor-Winfield 2.5-KVA, synchronous, AC resistance welder has been purchased and installed on the pilot line for experimental use in sealing of welded packages. A special low-mass air spring was designed and installed on the upper head to provide accurate control of weld pressure and electrode follow-through. Welding investigations will start next quarter as development packages are obtained.

Vacuum Oven and Dry Box
Figure 30



Encapsulation Welder
Figure 31

Section VI

THEORY OF OPERATION OF THE ASD SEMICONDUCTOR-NETWORK COMPUTER

6.1 Introduction

6.1.1 Purpose

The Aeronautical Systems Division (ASD) computer was designed and built to demonstrate the use of semiconductor networks in a digital application. This computer is shown in Figure 32. A conventional-component version of the computer was also built to serve as a basis for comparison. Figure 33 shows the relative size of these computers.

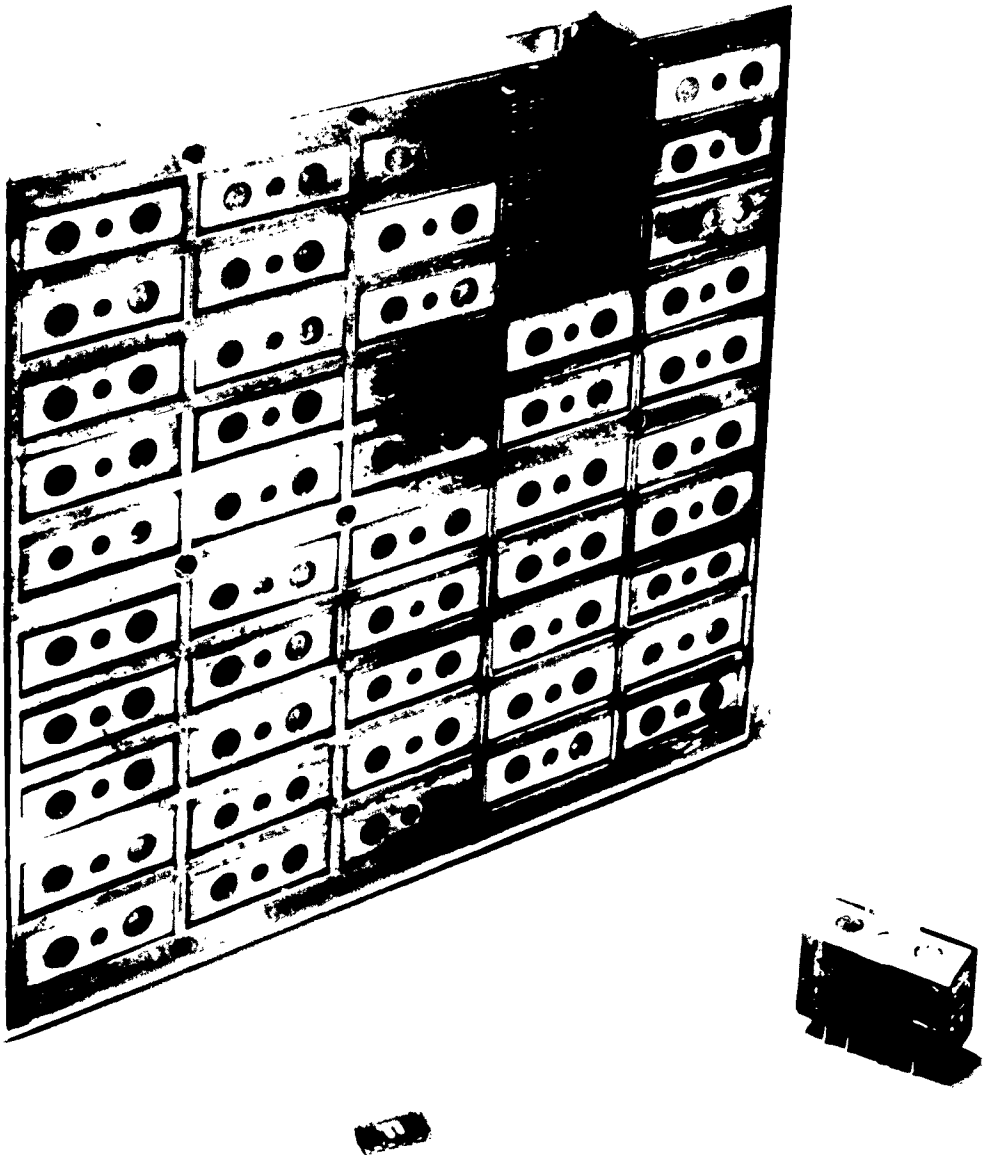
6.1.2 Specifications

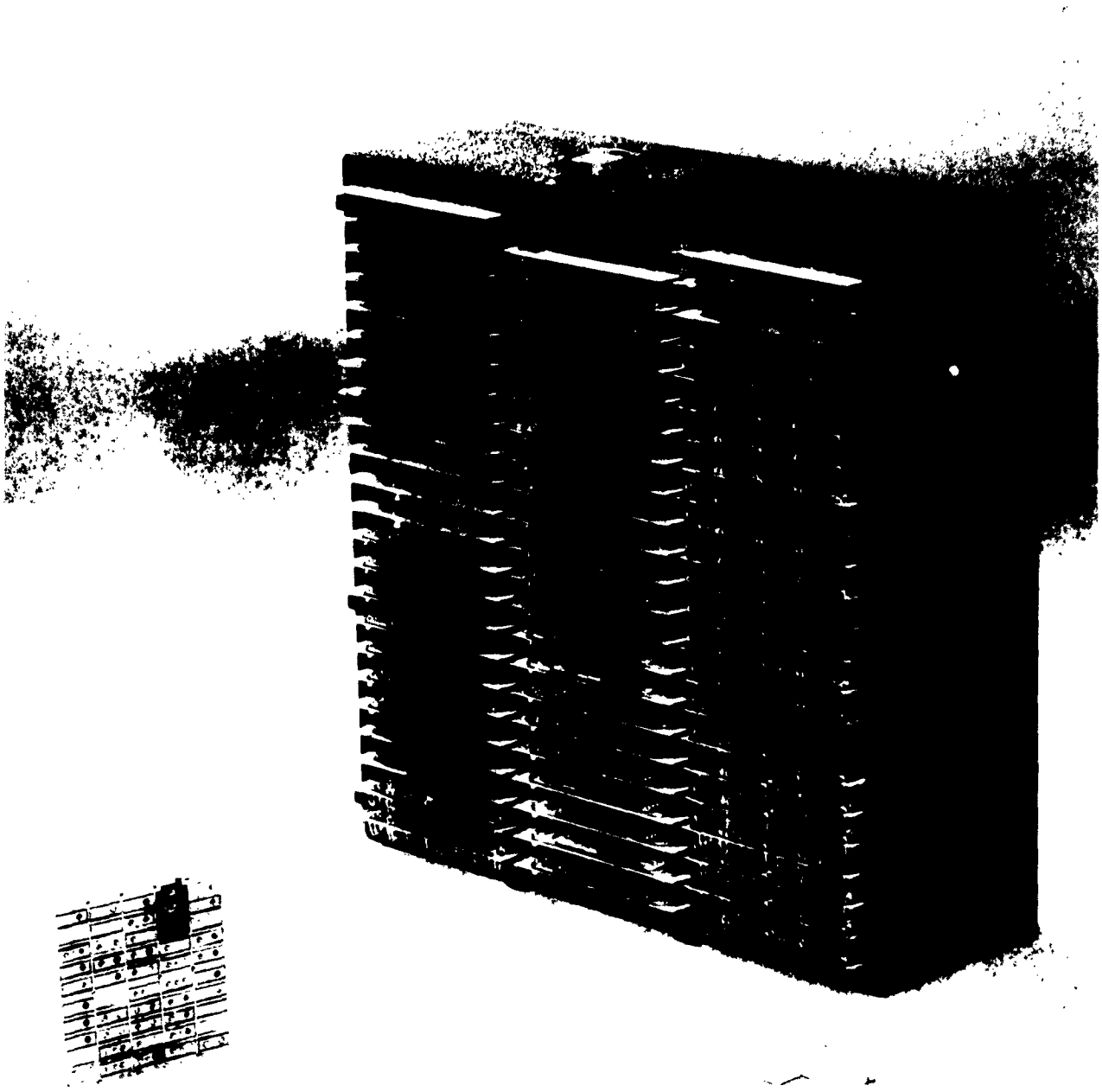
The basic demonstration equipment consists of two pieces, the manual control unit, Figure 34, and the computer. Auxiliary paper-tape equipment has also been provided for the computer.

The manual control unit is constructed of conventional components. It facilitates monitoring and control of the computer by the operator and provides a means for manual programming. The keys and the display provide communication between the machine and its operator. Figure 35 is a photograph of the keyboard of the manual control unit. A bilateral converter is included to allow the use of decimal input and output information with the binary computer. To provide additional computer capability, a 16-word extension of the instruction memory is also contained in the manual control unit. Power supplies for the manual control unit and the computer are included in the manual control unit.

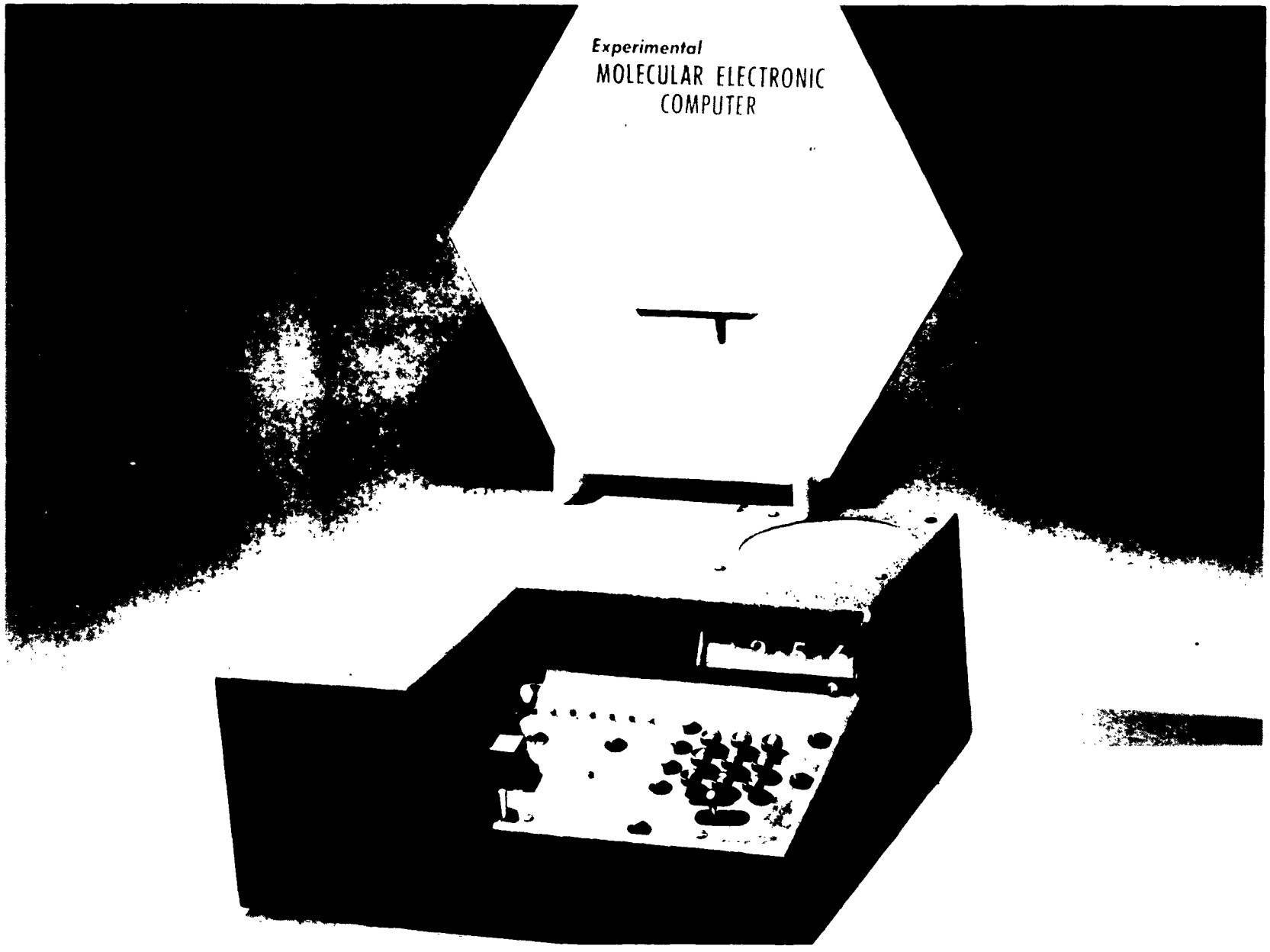
The computer is a serial, binary, fixed-point machine with an operand word length of 10 bits, plus sign. The logic is synchronous, being timed from an internal 200-kc clock. The instruction word contains eight bits. Of these eight bits, four bits are used for the operation code and four bits for the address code.

The computer can be programmed to operate as an electronic counterpart of a desk calculator. A special group of keys is provided on the manual control unit for this type of operation. The arithmetic operations: add, subtract, multiply, divide, and extract square root may be performed at will by the operator within the provisions of this computer program. The instruction memory has been extended to 32 words to accommodate the desk-calculator program, with the additional 16 words included in the manual control unit.



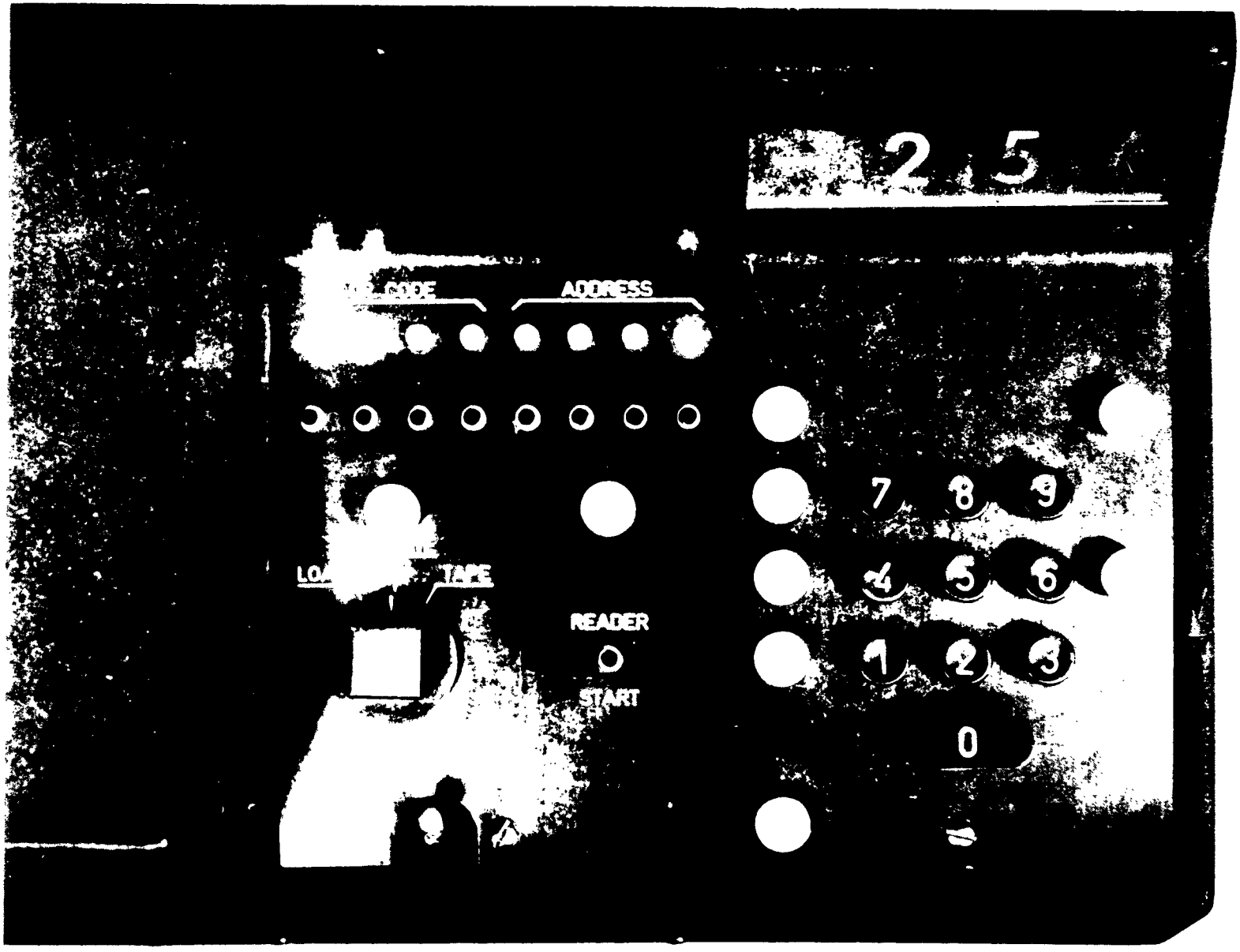


Size Comparison of Semiconductor-Network Computer
and Conventional-Component Computer
Figure 53

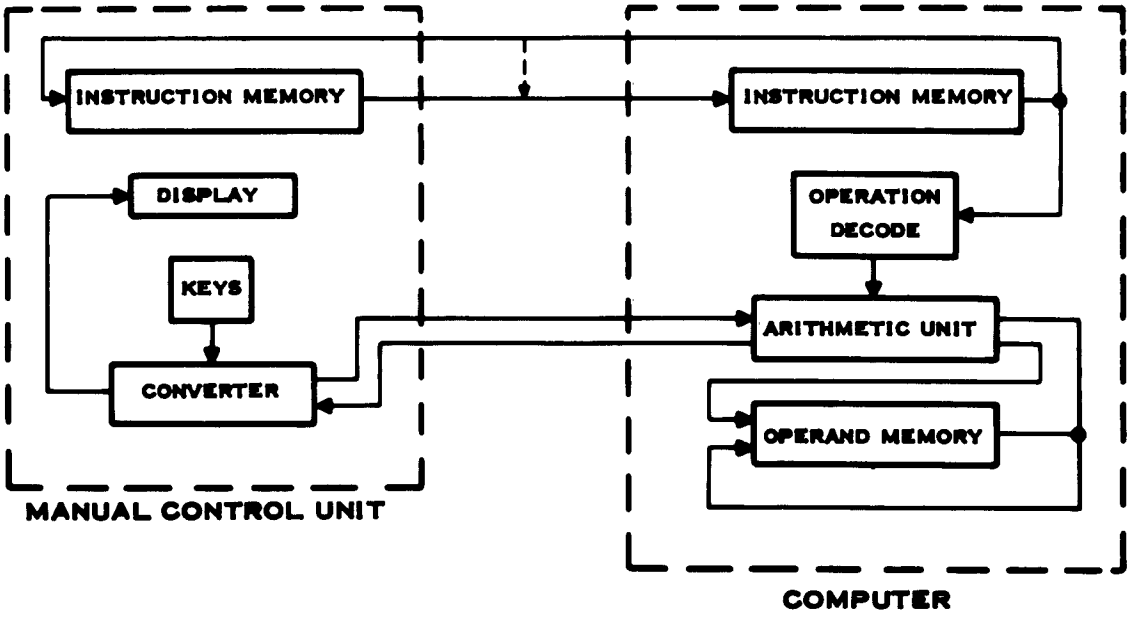


Manual Control Unit with Computer Display

Figure 31



Keyboard of Manual Control Unit
Figure 35



Computer and Manual Control Unit Block Diagram
Figure 36

6. 1. 3 Block Diagram and List of Operations

Figure 36 is a block diagram of the computer and manual control unit. Table 15 presents a list of computer operations.

Table 15. List of Operations

Mnemonic	Description
ADD	Add (n) to accumulator
CAD	Clear and add (n) to accumulator
SUB	Subtract (n) from accumulator
MUL	Multiply (n) by contents of accumulator, store product in accumulator
DIV	Divide contents of accumulator by (n), store quotient in accumulator
STR	Store accumulator in (n)
JPN	Jump on negative (n) words in instruction memory
JPZ	Jump on zero (n) words in instruction memory

Table 15. List of Operations (Continued)

Mnemonic	Description
JPU	Unconditional jump (n) words in instruction memory
OAT	Output accumulator to tape
OATS	Output accumulator to tape and stop
OAKS	Output accumulator to keyboard and stop
FAK	Fill accumulator from keyboard
LOM	Load memory from tape
SDN	Shift Operand memory to (n) and do nothing

6.2 Memory

6.2.1 Organization

The computer memory is comprised entirely of flip-flop shift registers. It is separated into two parts, the operand memory and the instruction memory. The operand memory is organized serially and has a capacity of 16 words. The instruction memory is word-organized and also has a capacity of 16 words.

6.2.2 Addressing Method

A relative-addressing scheme is used for both memories, permitting the memory capacity to be extended without modification of the instruction word format.

6.3 Control

6.3.1 Phases

The machine operation cycle may be separated into three distinct phases:

Phase 1—Pick up new instruction and begin address search, if required, or begin execution of operation

Phase 2—Search appropriate memory for specified address

Phase 3—Execute the specified operation.

6.3.1.1 Phase 1

Instructions are taken in sequence from the instruction memory. A new instruction is provided at bit time t_a upon entering the phase. The

address is loaded into the address counter during bit times t_a, t_b, t_c, and t_d. Phase 1 always requires only one word time for its completion. This one word time is devoted to beginning the address search, if required, or to beginning the operation execution.

6.3.1.2 Phase 2

If the current instruction requires an address search that has not been satisfied by the one word time of Phase 1, the machine cycle enters Phase 2. During this phase, the specified address is found. Phase 2 requires from 1 to 15 word times, depending upon the address.

6.3.1.3 Phase 3

When the current instruction requires operation time that has not been provided by the one word time of Phase 1, the machine cycle enters Phase 3. During this phase, execution of the specified operation is completed. Phase 3 requires from 1 to 999 word times, depending upon the operation.

6.3.2 Blocked State

A "stop" operation halts the machine cycle by blocking the normal control signals. The machine leaves the blocked state upon receipt of a "start" signal from the manual control unit.

The computer enters the blocked state under one other condition: when the memories are loaded from punched paper tape. During this time, the tape unit assumes control responsibilities and, upon completion of the loading operation, unblocks the machine.

6.3.3 Control Paths

For every word time that the computer is operating, the activity will be in one of the states shown in Figure 37.

Table 16. Control Paths

Path	Conditions for Using
A	Phase 1 includes one word time of address search, and further address search is required.
B	The specified address has been located as the result of a Phase 2 search
C	Phase 1 includes either one word time of address search or one word time of operation execution. Further address search is not required but further execution is required.

Table 16. Control Paths (Continued)

Path	Conditions for Using
D	Phase 3 has been terminated by completely executing the specified operation.
E	No address search is required and only one word time is required for executing the operation. This one word time is provided by Phase 1.
F	The instruction acquired by Phase 1 is OAKS, LOM, or OATS (with the presence of a READY signal from the tape punch).
G	The blocked state has been terminated by receipt of a signal from the tape unit or the manual control unit.

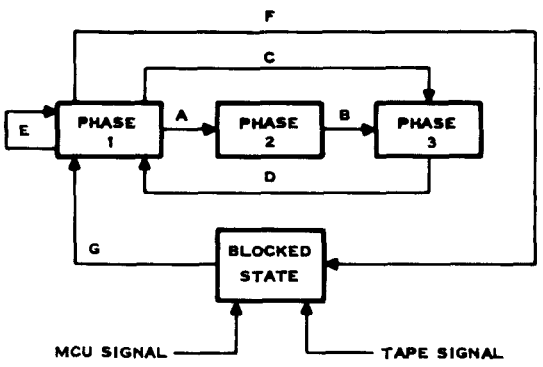
6.3.4 Instruction Sequencing

Instruction sequencing is accomplished by always executing the next instruction each time Phase 1 is entered. The transfer operations change the point of reference within the instruction memory such that the preceding rule need never be violated.

6.3.5 Addressing

The address field of each instruction is interpreted as pertaining to the operand memory, to the instruction memory, or to neither memory, depending upon the operation. The appropriate memory is then addressed by counting, with the address counter, the prescribed number of word times while the addressed memory is shifting. When the desired memory address has been found, as indicated by the address counter, execution of the operation is begun.

The interpretations given to the addresses listed for all operations are shown in Table 17.



Control Flow Diagram
Figure 37

Table 17. Address Interpretations

Operation	Address Interpretation
ADD	Operand memory
CAD	Operand memory
SUB	Operand memory
MUL	Operand memory
DIV	Operand memory
STR	Operand memory
JPN	Instruction memory

Table 17. Address Interpretations (Continued)

Operation	Address Interpretation
JPZ	Instruction memory
JPU	Instruction memory
OAT	No memory interpretation; must be zero address
OAKS	No memory interpretation; must be zero address
OATS	No memory interpretation; must be zero address
FAK	No memory interpretation; must be zero address
LOM	No memory interpretation; must be zero address
SDN	Operand memory.

The address counter is a minimum-logic, 15-state shifting counter with a forced, noncyclic sixteenth state. The relative addresses and their corresponding codes are given in Table 18.

Table 18. Relative Addresses

Relative Address	Code
0	0001
1	0011
2	0111
3	1111
4	1110
5	1101
6	1010
7	0101
8	1011
9	0110
10	1100
11	1001
12	0010
13	0100
14	1000
15	0000

The finding of a specified address is signaled by detection of the zero, or reference, address code pattern. The operation of the address counter is identical for addressing either the operand memory or the instruction memory.

6.3.6 Operation Decoding

Decoding of operations is not treated as a special case, but is included in the overall logic for the computer. Certain logical groupings of operations lend themselves to specific simplifications.

The operation codes are listed in Table 19.

Table 19. Operation Codes

Operation Mnemonic	Code
ADD	1111
CAD	0111
SUB	1011
MUL	1101
DIV	1001
STR	0101
JPN	0110
JPZ	0100
JPU	1010
OAT	0000
OAKS	1100
OATS	1110
FAK	1000
LOM	0010
SDN	0001

6.3.7 Arithmetic Operations

Addition and subtraction are executed in one word time each and, consequently, pose no peculiar control problems.

Multiplication requires ten word times plus two word times for register transfers, or a total of twelve word times. The multiplication counter, a twelve-state minimum-logic shifting counter, provides timing for the multiplication process.

Division is a variable-length operation and requires some form of detection in order to indicate completion. This is accomplished by detecting a change of sign in the accumulator. Because division is accomplished by successive subtraction, the sign change is a valid completion signal.

6.3.8 Storing in Memory

Storing is accomplished by replacing the contents of the addressed memory location with the data to be stored.

6.3.9 Input

Data may be channeled to the computer by using the accumulator as an input register or by loading the memories directly from punched tape. The operation FAK permits the accumulator to be filled from the manual control unit as a part of the normal machine cycle. Both memories may be filled from punched tape by the LOM operation.

6.3.10 Output

Computer output data may be presented either to the manual control unit or to the paper-tape unit. Output to the manual control unit is ordered by OAKS and concludes when the machine is stopped. The corresponding operation, which serves the paper-tape unit, is OATS. The OAT operation provides output to the paper tape unit without stopping the machine. An interlock is provided to assure completion of a given punching operation prior to acceptance of data for a new punching operation.

6.4 Arithmetic Section

6.4.1 General

The arithmetic section consists of a serial adder-subtracter with an additional shift register and logic for performing multiplication and division. Logic for detecting overflow, determining the resultant sign, sensing zero in the accumulator, and converting complement numbers to true form is also included in this unit. Negative numbers in the accumulator are always in the two's complement form, but are stored and used elsewhere in their true form. Figure 38 is a block diagram of the arithmetic section.

The arithmetic section is capable of performing on command the arithmetic operations: add, subtract, multiply, and divide for numbers of any sign combination, provided the resultant is not larger than the 10-bit capacity of the registers. All of these operations are exact. The division operation does not include round-off. The content of the

accumulator remains unchanged for instructions which do not pertain to the accumulator. The content of the operand memory is not changed or destroyed in performing the operations mentioned; however, it is advanced one word for each arithmetic operation that is executed.

6.4.2 Registers

The accumulator is used for storing the resultant of each arithmetic operation upon its completion. Basically, it is an 11-bit shift register including the sign bit. Gating is included either to set the sign bit independently or to remove it from the shift register, thereby forming a 10-bit register. Negative signs are represented by a logical one.

All the arithmetic operations use the accumulator to form the sum or difference, which is entered serially and shifted. Negative numbers are entered by subtracting so that they are always in the two's complement form in the accumulator.

The rules for setting the sign bit are given in Table 20. To eliminate the ambiguity of the sign of zero, the sign is always made positive for resultant answers of zero.

Table 20. Rules for Resultant Sign and Overflow

	Accumulator	0 0	1 1
	Sign Carry	0 1	0 1
Adding	Resultant Sign	0 0	1 0
	Overflow	0 1	0 0
Subtracting	Resultant Sign	0 1	1 1
	Overflow	0 0	Z 1

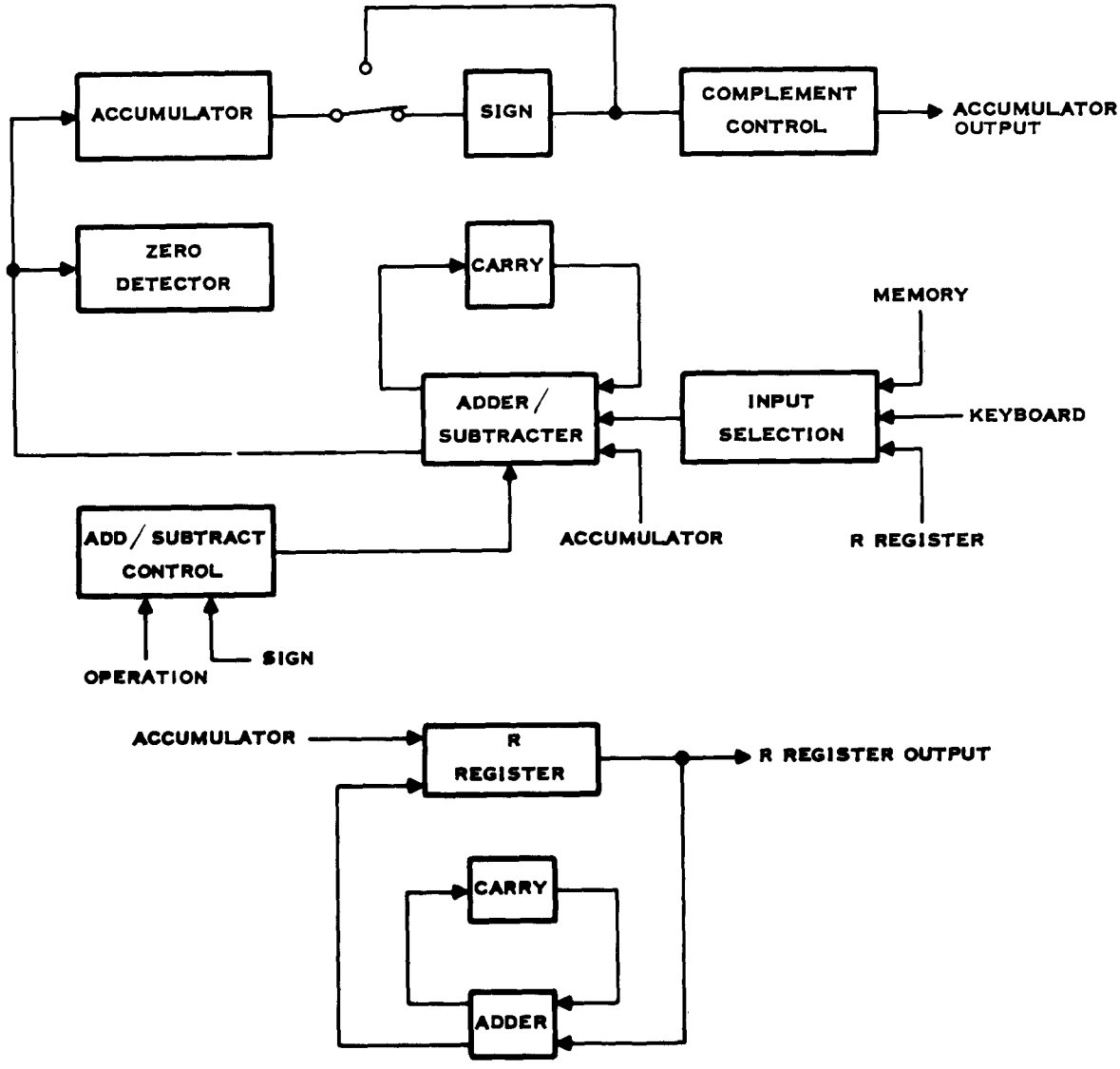
Note: Z indicates overflow if accumulator contains zero.

The R register is a 10-bit shift register without sign which is used for the multiply and divide operations. In multiplication, the multiplier is entered and then shifted right one bit per word time. The product is formed and inserted as the multiplier is shifted out.

For division, the R register accumulates the quotient. For each subtraction of the divisor from the dividend, a one is added to the register. The correct quotient is accumulated when sufficient subtractions have been made to reduce the dividend to zero.

6.4.3 Arithmetic Control

The add-subtract control is a flip-flop used to select either the summing or differencing process. The first, or sign bit, is always summed. Then the control is set to select the proper process for the



Arithmetic Section Block Diagram
Figure 38

successive bits, considering the operation and sign according to the rules in Table 21. In addition to selecting the process, this control is used in determining the final sign and overflow. For accumulator output operations, the sign is stored by the complement control and used to determine when the accumulator contents must be converted to true form.

The complement control converts the two's complement accumulator output of negative numbers to true form. The rule applied for this conversion is that starting with the least significant bit after the sign, all bits to and including the first "one" bit are transferred without change. All of the following more significant bits after the

Table 21. Rules for the Add Subtract Control

Operation	Sign of Addend or Subtrahend	Add-Subtract Flip-flop
Add	0	1
	1	0
Subtract	0	0
	1	1

Notes:

1. For sign, + = 0
   - = 1.

2. For add-subtract control, subtract = 0
   add = 1.

first "one" bit are inverted. For illustration, the representation of −10 with sign in both the two's complement and true form, as it would appear in this computer, is given below.

Two's complement: 1 1 1 1 1 1 0 1 1 0 1

True form: 0 0 0 0 0 0 1 0 1 0 1

The rule is mechanized by setting the complement control flip-flop with the first "one" following the sign bit. The complement control remains set through the particular word time and changes the gating so that all of the following bits are inverted. The add subtract control is used to store the accumulator sign for accumulator output operations.

The zero detector indicates whether or not the content of the accumulator is zero. This detector is set by the input to the accumulator, so that the indication is applicable to the content of the accumulator at the end of any word time. A zero detector output of logical one indicates that the content of the accumulator is not zero and a logical zero indicates a zero accumulator.

6.4.4 Addition and Subtraction Operations

Addition and subtraction are the basic processes used for performing operations pertinent to the arithmetic section. Organizations of the logic for completing operations ADD and SUB is according to process rather than operation, the proper process being selected by applying the rules of algebra to the operation and to the sign of the number to be added or subtracted (Table 21).

The contents of the accumulator and of the last memory word are added or subtracted by shifting both registers while serially adding or subtracting their outputs according to the rules in Table 22. The

Table 22. Rules for Adding and Subtracting

Inputs	Accumulator	0 0 0	0 1 1	1 1
	Memory	0 0 1	1 0 0	1 1
	Carry	0 1 0	1 0 1	0 1
Add	Sum	0 1 1	0 1 0	0 1
	Carry	0 0 0	1 0 1	1 1
Subtract	Difference	0 1 1	0 1 0	0 1
	Borrow	0 1 1	1 0 0	0 1

duration of the shifting is 11 bit times (the number of active bits in a word time). The result is entered into the accumulator during this word time of shifting. The final sign and overflow (if any) are set on the bit time following the operation according to the rules in Table 23.

Table 23. Addition-Subtraction Sign Control and Overflow Conditions

Operation	Condition	Initial Sign		Process	Final		
		Acc.	Memory		Carry	Sign	Overflow
Add	Acc > (n)	+	+	Addition	*	+	C
	Acc < (n)				*	+	C
	Acc = (n)				*	+	C
	Acc > (n)	-	+	Addition	No	-	None
	Acc < (n)				Yes	+	None
	Acc = (n)				No	-	None
	Acc > (n)	+	-	Subtraction	No	+	None
	Acc < (n)				Yes	-	None
	Acc = (n)				No	+	None
	Acc > (n)	-	-	Subtraction	*	-	C or Z
	Acc < (n)				*	-	C or Z
	Acc = (n)				*	-	C or Z
Subtract	Acc > (n)	+	+	Subtraction	No	+	None
	Acc < (n)				Yes	-	None
	Acc = (n)				No	+	None

Table 23. Addition-Subtraction Sign Control and Overflow Conditions (Continued)

Operation	Condition	Initial Sign		Process	Final		
		Acc.	Memory		Carry	Sign	Overflow
	Acc > (n)	–	+	Subtraction	*	–	C or Z
	Acc < (n)				*	–	C or Z
	Acc = (n)				*	–	C or Z
	Acc > (n)	+	–	Addition	*	+	C
	Acc < (n)				*	+	C
	Acc = (n)				*	+	C
	Acc > (n)	–	–	Addition	No	–	None
	Acc < (n)				Yes	+	None
	Acc = (n)				No	–	None

NOTES: * Indicates carry is indeterminate
C Indicates overflow if carry is one
Z indicates overflow if accumulator is zero
(n) indicates contents of n, the addressed memory location

For clarification, the sequence of events occurring during the execution portion of add and subtract commands is presented below:

Table 24. Sequence of Events for Add and Subtract Commands

Bit Time	Events
t_d	Add-subtract control set to add
t_1	Accumulator shift pulses started Accumulator sign re-entered into accumulator Add-subtract control set or reset according to the rules of Table 21
t_2 through t_{11}	Sum or difference of each bit is entered into the accumulator according to the rules of Table 22. Carry is set according to the rules of Table 22. Accumulator shift pulses are stopped after t_{11}.
t_a	Accumulator and carry examined for overflow and final sign set according to the rules of Table 23.

6.4.5 Multiplication Operation

The multiplication of two numbers is accomplished by successive additions and shifts. The complete process requires twelve word times. For illustration, an example of the multiplication operation on a similar computer with a reduced word length is shown in Table 25.

Table 25. Multiplication Example: (+2) x (+3) = +6

Bit Time	Memory	Accumulator	R Register	Operation
0	0 1 0 0	0 1 1 0	0 0 0	Initial Values
1	0 0 1 0	0 0 1 1	No shift	Transfer accumulator contents without sign to R register.
2	0 0 0 1	0 0 0 1	1 0 0	
3	1 0 0 0	0 0 0 0	1 1 0	
4	0 1 0 0	0 0 0 0	0 1 1	
1	0 0 1 0	0 0 0 0	No	Add multiplicand to accumulator if the least significant bit of the R register is one; add nothing if zero. Accumulator is shortened by one bit.
2	0 0 0 1	1 0 0 0	shift	
3	1 0 0 0	0 1 0 0	pulses	
4	0 1 0 0	0 0 1 0	0 0 1	
1	0 0 1 0	1 0 0 0	No	
2	0 0 0 1	1 1 0 0	shift	
3	1 0 0 0	0 1 1 0	pulses	
4	0 1 0 0	0 0 1 0	1 0 0	
1	0 0 1 0	1 0 0 0	No	
2	0 0 0 1	0 1 0 0	shift	
3	1 0 0 0	0 0 1 0	pulses	
4	0 1 0 0	0 0 0 0	1 1 0	
1	Next	0 0 0 0	No shift	Accumulator input set with final sign. Transfer contents of R register to accumulator, subtracting if final sign is negative.
2	Operand	0 0 0 0	0 1 1	
3	Shifted	1 0 0 0	0 0 1	
4	In	1 1 0 0	0 0 0	

During the first word time, the multiplier without sign is transferred from the accumulator to the R register. The accumulator is cleared of all but the sign, which is stored until the last word time of multiplication. The multiplicand is recirculated in the last word position of the memory.

The actual multiplication is achieved during the next ten word times. For this period the sign bit is removed from the accumulator, resulting in a 10-bit register which receives 11 shift pulses each word time. This causes a right shift of one bit per word time. The R register is also shifted right one bit at the end of each word. The multiplicand without sign is added to the accumulator for each word time that the least significant bit of the R register is one. This addition is completed on bit time t_{10} of each word time. A zero is inserted in the accumulator, and the least significant bit of the accumulator is transferred to the R register on bit time t_{11}. The product is, therefore, formed in the R register.

The product is transferred from the R register to the accumulator during the last word time. The final sign is set at the beginning of this word time. The complement is formed by subtracting the product from zero when entering negative numbers.

Overflow is indicated when the accumulator has a remainder at the beginning of the last word time.

6.4.6 Division Operand

Division of two numbers is accomplished by successive reduction of the dividend (accumulator), by the divisor, until the accumulator becomes zero or changes sign. The quotient is formed by counting the number of reductions required. The number of word times required to complete the divide operation is two more than the value of the quotient. Round-off is not included, so the quotient is simply the number of whole times the divisor will go into the dividend. For illustration, an example of division on a similar computer with a shortened word length is shown in Table 26.

Table 26. Division Example: (+7) / (+2) = +3

Assume 3 bits plus sign for the operand word length.

Bit Time	Memory	Accumulator	Accumulator Carry	R Register	R Carry	Operation
0	0 1 0 0	1 1 1 0	0	1 1 1	0	
1	0 0 1 0	0 1 1 1	0	No shift	1	Subtract divisor from accumulator for positive dividends. Add if negative; clear R register.
2	0 0 0 1	1 0 1 1	0	0 1 1	0	
3	1 0 0 0	0 1 0 1	0	0 0 1	0	
4	0 1 0 0	1 0 1 0	0	0 0 0	0	
1	0 0 1 0	0 1 0 1	0	No shift	1	
2	0 0 0 1	1 0 1 0	0	1 0 0	0	
3	1 0 0 0	1 1 0 1	1	0 1 0	0	
4	0 1 0 0	0 1 1 0	0	0 0 1	0	
1	0 0 1 0	0 0 1 1	0	No shift	1	
2	0 0 0 1	1 0 0 1	0	0 0 0	1	
3	1 0 0 0	0 1 0 0	0	1 0 0	0	
4	0 1 0 0	0 0 1 0	0	0 1 0	0	
1	0 0 1 0	0 0 0 1	0	No shift	1	
2	0 0 0 1	1 0 0 0	0	1 0 1	0	
3	1 0 0 0	1 1 0 0	1	1 1 0	0	
4	0 1 0 0	1 1 1 0	1	0 1 1	0	
1	Shifts	0 1 1 1	0	No shift	1	Acc. input set with final sign. Transfer contents of R register to accumulator, subtracting if final sign is negative.
2	in	1 0 1 1	0	0 0 1	1	
3	next	1 1 0 0	0	0 0 0	1	
4	operand	0 1 1 0	0	1 0 0	0	

During the divide operation, the dividend sign is recirculated in the accumulator. This is done by adding the first bit (sign) to zero and entering the sum. On the following bits, the divisor and the dividend are added or subtracted as required to reduce the accumulator value. The divisor is recirculated in the last word position of the memory. In order always to lessen the value in the accumulator, the divisor is subtracted from positive dividends and added to negative ones, since negative dividends are in complement form in the accumulator. The add-subtract control is set according to the above rule on each word after the sign bit is entered.

This process of reduction is repeated until the accumulator carry is a logical one after the end of the word. This carry occurs when positive dividends are reduced past zero or when negative dividends either become zero or positive. The carry initiates the last divide word time. During this word time, the final sign is set into the accumulator, and the quotient is transferred from the R register to the accumulator.

The quotient is formed in the R register by resetting the register to zero on the first word time of divide, and then setting its carry to one at the beginning of each succeeding word until the last word time. The loss of a count during the first word is corrected by the count received during the word time that the accumulator is reduced past zero. In the case of negative dividends being reduced to zero, a count must be added to the final answer. This is done by setting the accumulator carry to one at the beginning of the last word, when this situation is detected.

Overflow is indicated when the R register is full. The carry of that register is used to indicate overflow. Dividing by zero is the only division case that can produce an overflow.

6.5 Descriptive List of Flip-Flops

Table 27. Descriptive List of Flip-Flops

Flip Flop	Description
1-165	First 15 words of operand memory
166-176	Last word of operand memory
201-216	Instruction-memory 4th address bit
217-232	Instruction-memory 3rd address bit
233-248	Instruction-memory 2nd address bit
249-264	Instruction-memory 1st address bit
265-280	Instruction-memory 4th operation bit

Table 27. Descriptive List of Flip-Flops (Continued)

Flip-Flop	Description
281-296	Instruction-memory 3rd operation bit
297-312	Instruction-memory 2nd operation bit
313-328	Instruction-memory 1st operation bit
401-410	Accumulator
411	Accumulator sign
412	Accumulator carry
501-510	R register
512	R-register carry
601	Add-subtract control
602	Complement control
603	Zero detector
750-753	Address counter
761-776	Timing distributor
780-785	Multiply counter
801	Accumulator shift control
802	Operand-memory shift control
803	Last-operand-word shift control
804	Instruction-memory shift control
805	Multiply-counter shift control
806	Address-counter shift control
807	R-register shift control
808	Blocked-state control
809	Load address counter
810	Last divide word time control
811	Jump-address search control
812	First divide word time control

6.6 Manual Control Unit

The flip-flop, gate, and driver circuits used in the manual control unit are of the same types as those used in the conventional-component

computer. However, in addition to these three types, a push-button synchronization circuit and a lamp-driver circuit are required. Diagrams of these circuits are given in Figures 39 and 40, respectively.

The numbers being handled by the manual control unit are stored in a 12-bit shift register. When storing a decimal number this register may be thought of as three 4-bit modules, each of which is capable of storing one binary-coded decimal digit. All transfers are handled by the module in the least-significant-digit position.

Read-in from the keyboard is effected by shifting the register eight places end around to the right, moving the decimal digits previously contained one place to the left, then shifting the register twelve places to the right and parallel-transferring the new number into the last module on the first shift pulse. If the most significant bit contains a number other than zero when an entry is started, a gate causes the eight-place shift to be replaced by a twelve-place shift and sets the input to the register to zero, clearing the register before entry.

Binary-to-decimal conversion is accomplished by the BI-DEC method, which is as follows: If a binary number is shifted to the left, its value is doubled. The shifting of a 1 from the fourth to the fifth place of a binary number represents an increase from 8 to 16. If the first four bits of a shift register are considered to be a binary-coded decimal module, a carry from one module to the next should represent an increase from 8 to 10. To correct a number to binary-coded decimal (bcd) form, six should be subtracted from it each time a carry from one module to the next occurs. Because it is easier to mechanize, the carry is anticipated by one shift pulse, and the resulting rule is: When the number in a module exceeds 5, subtract 3 from it as the shift is made. Decimal-to-binary conversion is accomplished by reversing this principle. The register is shifted right and 3 is added each time the number exceeds 8.

In the manual control unit, left shift was omitted to reduce the logic circuitry required. Left shifts are effected by right-shifting end-around eleven places. End-around shifting preserves the unconverted portion of the number during conversions.

When a number is to be converted, it is shifted right eleven or thirteen places per word time, according to which type conversion is taking place. The number is tested twice each word time at the bit times when a carry is possible between the first and second or second and third modules. If a carry is detected, a gate is energized for adding or subtracting 3. Seven word times are required for decimal-to-binary conversion and eight are required for binary-to-decimal conversion.

The sign bit is stored in a flip-flop which is modified or sampled during the first bit of a word time when transfers to and from the computer are taking place.

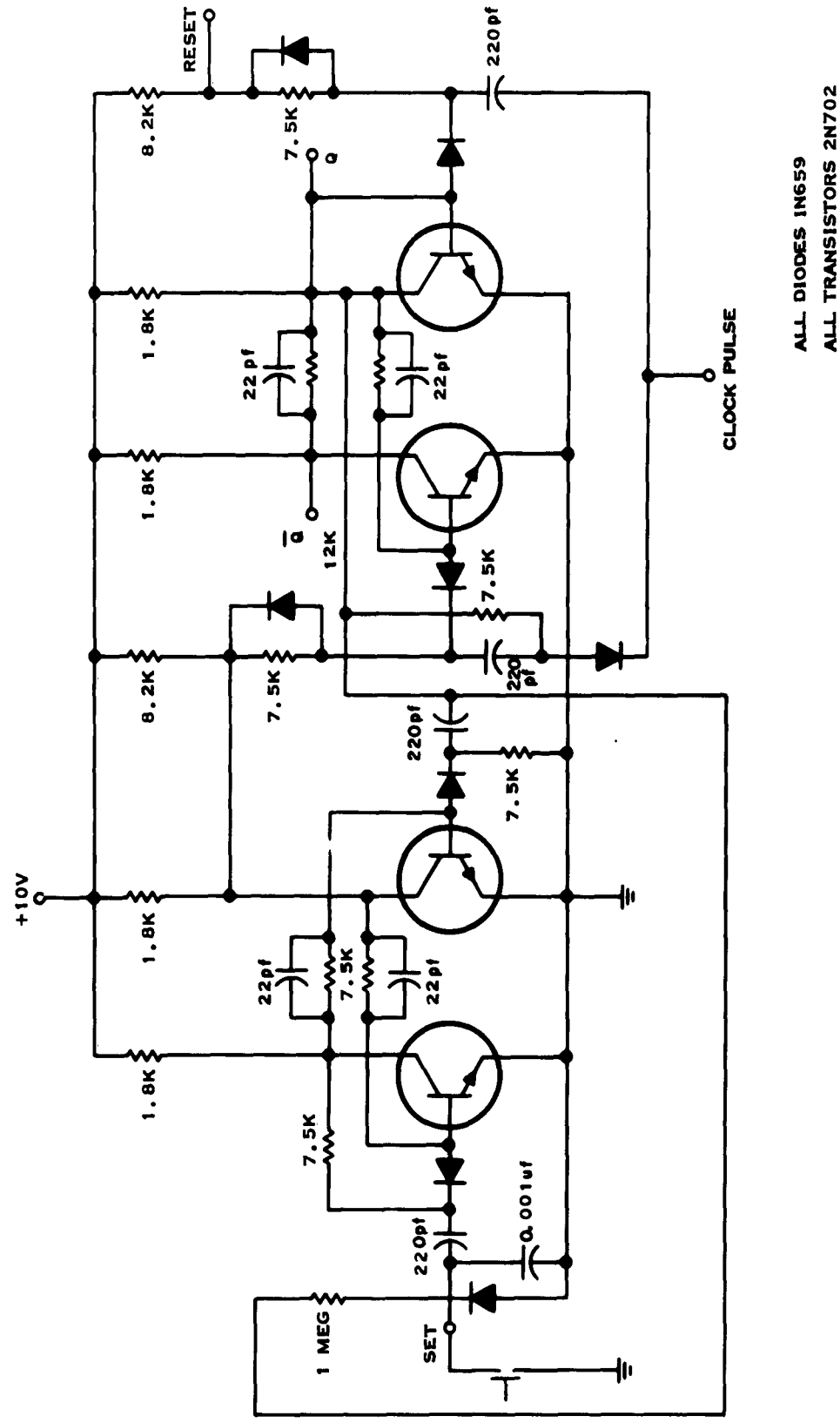
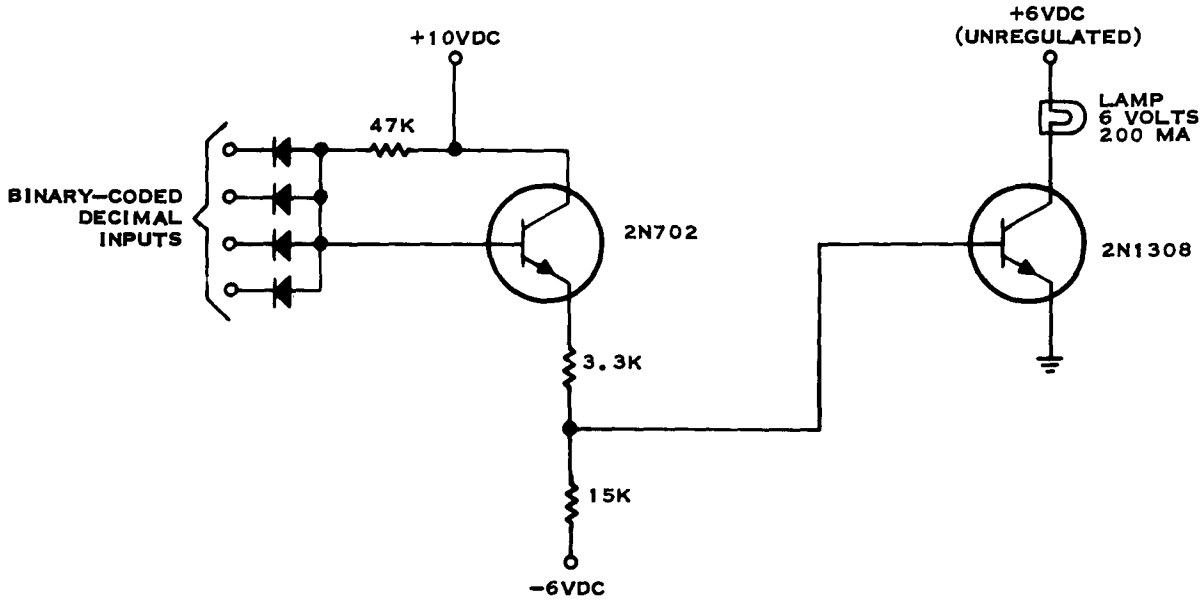


Diagram of Push-Button Synchronization Circuit
Figure 39



Lamp-Driver Circuit
Figure 40

The manual control unit also contains a provision for starting the timing distributor in the computer. When the clear (CLR) button is pressed, a pusn-button pulse circuit is set, clearing the ring counter. When the button is released, another push-button pulse circuit is set for one bit time, starting the distributor. The clearing signal resets both pulse circuits simultaneously.

The contents of the instruction-memory flip-flops in the computer are modified by grounding the collectors through diodes and push-button switches.

Push-buttons are provided for calling up specific subroutines which may have been stored in the instruction memory. For the desk-calculator program, these subroutines are "add," "multiply," "divide," and "square root." The names of the subroutine push-buttons correspond with the subroutines of this program.

The operand memory is loaded from the keyboard in a manner similar to filling the accumulator. After converting the number to binary form and serially transferring it to the operand memory, the manual control unit reconverts the number to decimal form for readout.

6.7 Paper-Tape Control Unit

6.7.1 Paper-Tape-Punch Control

6.7.1.1 Automatic Punch Operation

The paper-tape control unit was designed to accept an 11-bit binary word and automatically transfer this information to paper tape. This information can originate in either the computer or the manual control unit. The paper-tape control unit treats the two sets of information identically. The desired input is manually selected by positioning the mode switch.

If it is desirable to record information contained in the computer, this information must be transferred to the accumulator. The accumulator contents can then be recorded on tape upon command from the computer. The mode switch must be in the OPERATE position for this type of operation.

Tape may be automatically prepared in the proper format for operand memory loading with the mode switch in the LOAD position. This facilitates the preparation of input tapes for the computer.

Upon command from the selected input unit, the contents of the applicable shift register are shifted into an 11-bit holding register. When this register is filled, the punch clutch is engaged. Each revolution of the punch generates a clock pulse. This clock pulse is gated to the 11-bit holding register and the information is shifted out to the code magnet puller.

After 11 punch cycles, the punch clutch is disengaged and a "ready" signal is given to the computer indicating the ability to accept new information.

Operands are recorded on the first channel of the tape. The first bit recorded is the sign bit followed by a 10-bit binary word, having the least-significant bit first. A hole is punched in the second channel opposite the sign bit for word-orientation purposes.

6.7.1.2 Manual Tape Operation

With the mode selector switch in the TAPE position, tape may be punched manually. The code magnet gates are enabled by the instruction-memory load switches. The enabled code magnets and the clutch magnet are energized by the ENTER (ENT) switch. Each punch cycle resets the magnet pullers and gates.

Paper tape may also be copied in this mode. Tape inserted in the reader is reproduced. The reader brushes are parallel with the instruction-memory load switches and the reader advances with each

punch cycle. This requires that the brush head be lowered only when tape is to be reproduced or loaded into the computer.

6.7.2 Paper-Tape-Reader Control

Information may be loaded into the operand memory or the instruction memory, or both, from tape. If both memories are to be loaded, the operand memory is the first to be loaded.

The loading cycle can be initiated manually while in the "load" mode or can be initiated upon command from the computer while in the "operate" mode. The load operation is identical for both cases.

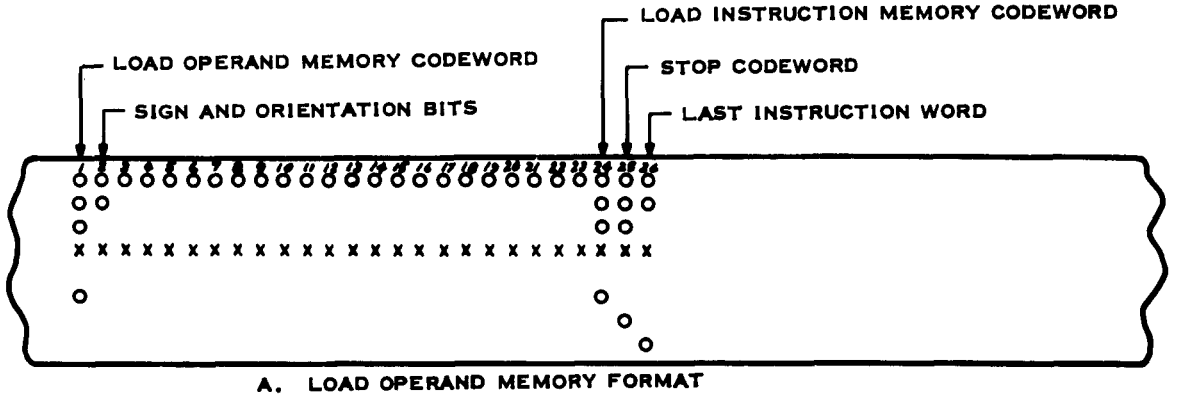
The "initiate" signal energizes the tape reader. The first frame of information is a code word indicating the load operation. Following the load-operand-memory (LOM) code word are the operand words to be loaded. They are in a serial format in the first tape channel. (See Figure 41). When loading, the operand-memory input gate is enabled. After each tape advance, a shift pulse is generated. This pulse shifts the information under the brush head into the operand memory.

Since the reader brushes are in parallel with the instruction-memory load switches, it is necessary to clear the instruction memory before new information is introduced under the brush head. This signal is generated during the interval between tape information frames.

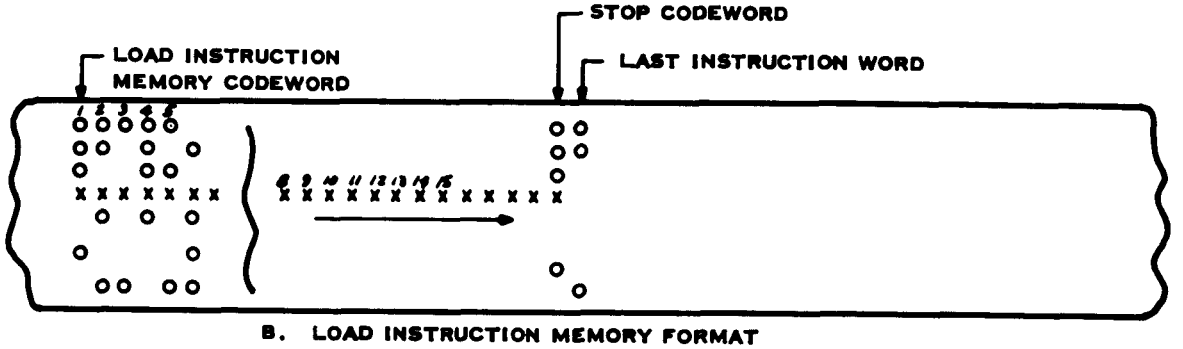
Transferring from the operand-memory load operation to the instruction-memory load operation is accomplished by following the last bit of operand information with a code word indicating the instruction-memory load operation. (See Figure 41.) This code word is followed by the 8-bit instruction words. To stop the loading operation a third code word is utilized. This word generates a signal which stops the tape reader and, if the mode switch is in the OPERATE position, a signal is generated which starts the computer.

During the load-instruction-memory procedure, stop signals and clear signals are generated. These signals occur in the interval when no information is under the brush head. This timing is necessary to prevent erroneous information from entering the instruction memory. To prevent the "stop" code word from being introduced into the instruction memory, the code word must precede the last instruction word. (See Figure 41.) During this next-to-last word time, the instruction memory is cleared but not stepped.

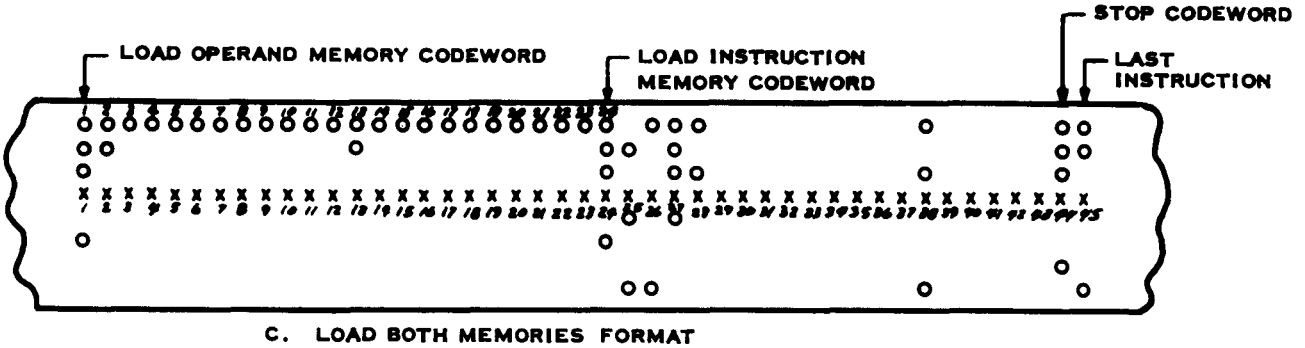
If it is desired to load the operand memory only, it is still necessary to go through the load-instruction-memory code word and the last instruction-memory word. This step is necessary to reconstruct the last word of instruction. (See Figure 41.) This word is destroyed during the load-operand-memory operation



A. LOAD OPERAND MEMORY FORMAT

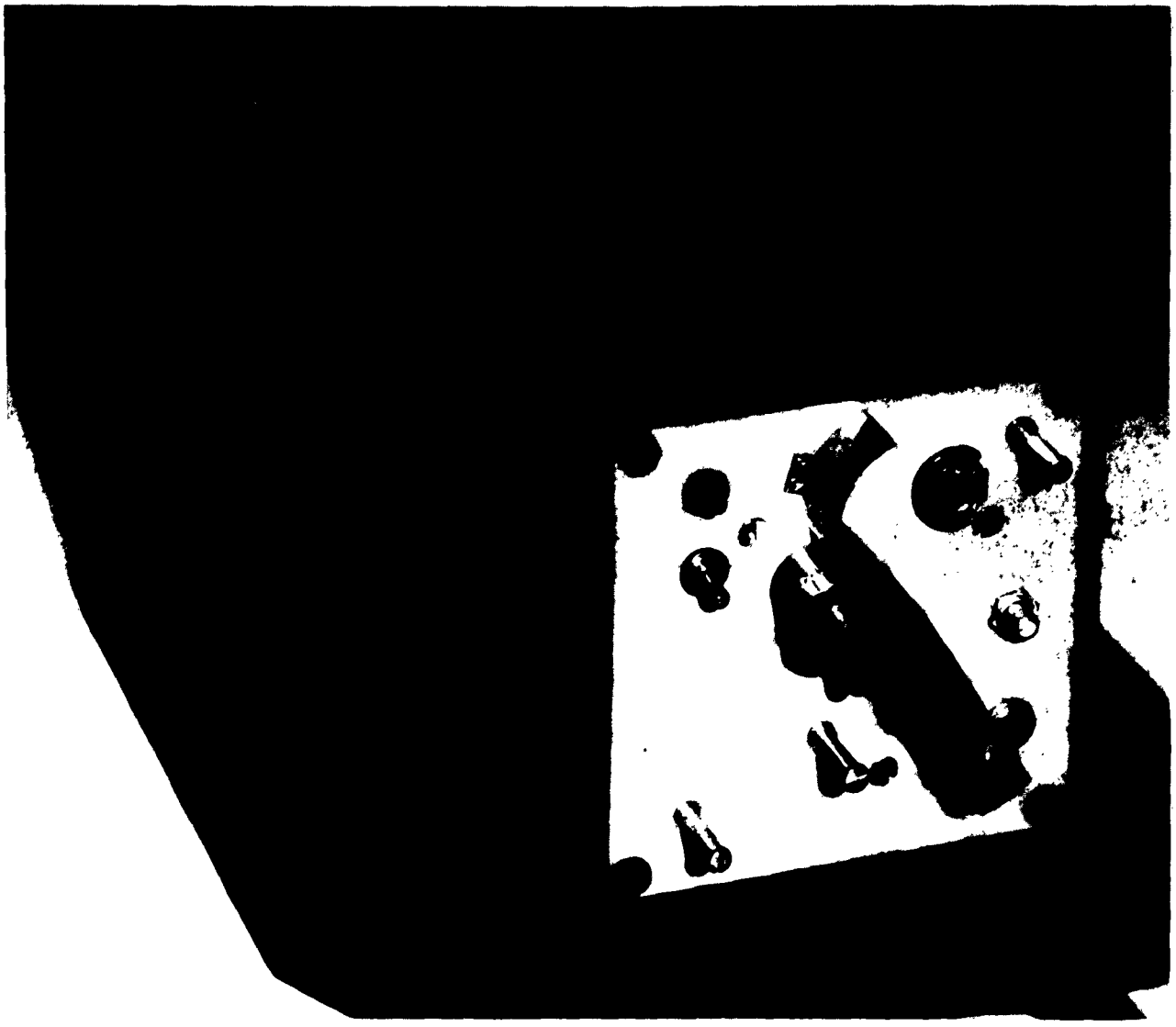


B. LOAD INSTRUCTION MEMORY FORMAT



C. LOAD BOTH MEMORIES FORMAT

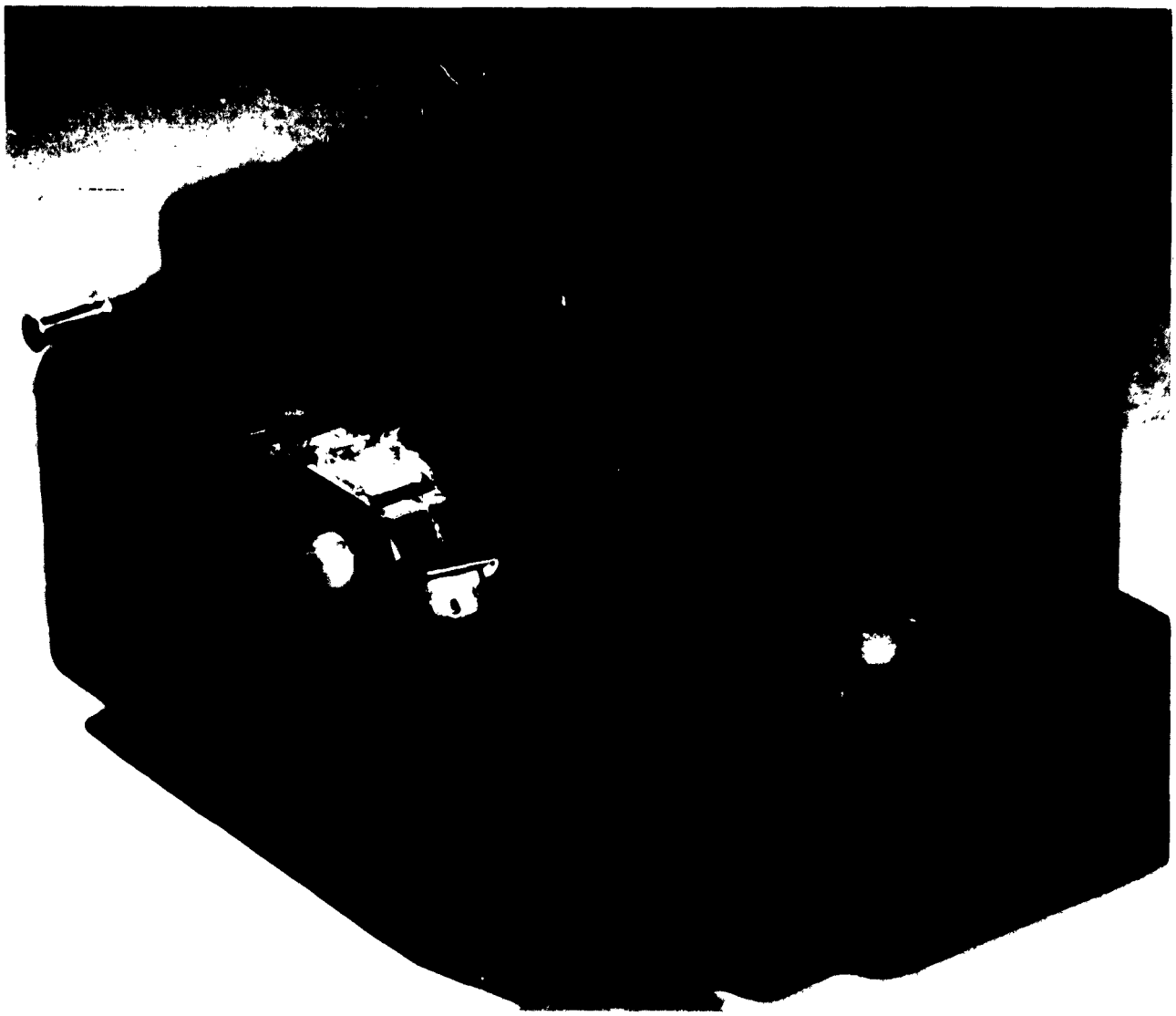
Tape-Loading Formats
Figure 41



Paper-Tape Reader and Control Unit
Figure 42

The tape reader stops on a blank tape frame and thus prohibits destroying the contents of the instruction memory while the computer is in operation.

Figure 42 is a photograph of the paper-tape reader and control unit. The punch is illustrated in Figure 43.



Paper-Tape Punch
Figure 43

6.8 Programming

6.8.1 Introduction

The programming schedule which should be used for this computer is as follows:

a. Prepare a flow diagram in terms of the machine operations.

b. Arrange the program on Programming Sheets (Figure 44).

c. Write the machine code for the program on Coding Sheets (Figure 45).

PROGRAMMING SHEET
SQUARE-ROOT PROGRAM

A X
B −1
C −2
D A1, A2, A3...

OPERATION	ADDRESS	INSTRUCTION NO.	OPERAND RELATIVE ADDRESS															
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDN	0	1	0	N	M	L	K	J	I	H	G	F	E	D	C	B	A	P
FAK	—	2	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
STR	0	3	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
CAD	0	4	A	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B
STR	1	5	B	A	P	O	N	M	L	K	J	I	H	G	F	E	D	C
ADD	12	6	D	C	B	A	P	O	N	M	L	K	J	I	H	G	F	E
JPN	4	7	A	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B
STR	15	8	A	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B
CAD	2	9	A	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B
ADD	14	10	D	C	B	A	P	O	N	M	L	K	J	I	H	G	F	E
JPU	9	11	C	B	A	P	O	N	M	L	K	J	I	H	G	F	E	D
CAD	2	12	A	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B
SUB	13	13	D	C	B	A	P	O	N	M	L	K	J	I	H	G	F	E
DIV	0	14	B	A	P	O	N	M	L	K	J	I	H	G	F	E	D	C
JPU	3	15	C	B	A	P	O	N	M	L	K	J	I	H	G	F	E	D
		16																
		17																
		18																
SDN	11	19	C	B	A	P	O	N	M	L	K	J	I	I	G	F	E	D
JPU	11	20	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A	P
SDN	14	21	C	B	A	P	O	N	M	L	K	J	I	H	G	F	E	D
JPU	14	22	B	A	P	O	N	M	L	K	J	I	H	G	F	E	D	C
		23																
		24																
		25																
		26																
		27																
		28																
		29																
		30																
		31																
OAKS		32	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A	P

Programming Sheet
Figure 44

CODING SHEET

INSTRUCTION NO.	MNEMONIC	INSTRUCTION CODE	ADDRESS CODE	ADDRESS
1	SDN	0001	0001	0
2	FAK	1000	0001	0
3	STR	0101	0001	0
4	CAD	0111	0001	0
5	STR	0101	0011	1
6	ADD	1111	0010	12
7	JPN	0110	1110	4
8	STR	0101	0000	15
9	CAD	0111	0111	2
10	ADD	1111	1000	14
11	JPU	1010	0110	9
12	CAD	0111	0111	2
13	SUB	1011	0100	13
14	DIV	1001	0001	0
15	JPU	1010	1111	3
16				
17				
18				
19	SDN	0001	1001	11
20	JPU	1010	1001	11
21	SDN	0001	1000	14
22	JPU	1010	1000	14
23				
24				
25				
26				
27				
28				
29				
30				
31				
32	OAKS	1100	0001	0

NOTE: FOR SQUARE-ROOT PROGRAM

Coding Sheet
Figure 45

d. Prepare Paper-Tape-Punch Data Sheets (Figure 46) for preparing input tapes, if required.

6.8.2 General Programming Information

The operations which address the operand memory are ADD, CAD, SUB, MUL, DIV, STR, and SDN. When these operations are executed, they advance the operand memory one word. The total operand memory shift for instruction words using these operations is n + 1, where n is the instruction address.

Jump addresses are interpreted as being the number of consecutive instructions that are omitted from the instruction interpretation-execution process when the jump occurs.

When the computer is started from the manual control unit, the number displayed immediately prior to starting is available for acceptance by the accumulator only during the second word time after starting. This is the only time that the FAK operation may be used.

6.8.3 Example of Programming

As an example, a program for extracting square roots will be developed. Consider the sequence

$1, 3, 5, 7, \text{---} a_n \text{---}$

where $a_n = 2n-1$.

If the members of this sequence are successively subtracted from the square root argument, X, until the argument becomes negative on the p^{th} subtraction, then

$$m = \frac{a_p - 1}{2}$$

where $m = \sqrt{X}$ to the largest integral value

a_p = last member of sequence used.

By this technique, the square root of 25 may be found as follows:

$a_1 = 1$

$a_2 = 3$

$a_3 = 5$

$a_4 = 7$

$a_5 = 9$

$a_6 = 11$

$X = 25$

PAPER-TAPE-PUNCH DATA SHEET

NO.	DESCRIPTION	CODE		NO.	DESCRIPTION	CODE	
1	LOAD OP	1110	1000	176	JPU	1010	1001
2, 12	-1			177	SDN	0001	1000
13, 23	-2			178	JPU	1010	1000
24, 34	0			179			
35, 45	0			180			
46, 56	0			181			
57, 67	0			182			
68, 78	0			183			
79, 89	0			184			
90, 100	0			185			
101, 111	0			186			
112, 122	0			187			
123, 133	0			188	STOP	1110	0010
134, 144	0			189	OAKS	1100	0001
145, 155	0						
156	LOAD INST.	1110	0100				
157	SDN	0001	0001				
158	FAK	1000	0001				
159	STR	0101	0001				
160	CAD	0111	0001				
161	STR	0101	0011				
162	ADD	1111	0010				
163	JPN	0110	1110				
164	STR	0101	0000				
165	CAD	0111	0111				
166	ADD	1111	1000				
167	JPU	1010	0110				
168	CAD	0111	0111				
169	SUB	1011	0100				
170	DIV	1001	0001				
171	JPU	1010	1111				
172							
173							
174							
175	SDN	0001	1001				

LOAD OP. 11101000
LOAD INST. 11100100
STOP 11100010

COMMENTS:

Paper-Tape-Punch Data Sheet
Figure 46

$$X - a_1 = 24$$

$$X - a_1 - a_2 = 21$$

$$X - a_1 - a_2 - a_3 = 16$$

$$X - a_1 - a_2 - a_3 - a_4 = 9$$

$$X - a_1 - a_2 - a_3 - a_4 - a_5 = 0$$

$$X - a_1 - a_2 - a_3 - a_4 - a_5 - a_6 = -11$$

$$a_p = a_6 = 11$$

$$m = \frac{a_p - 1}{2} = \frac{11-1}{2} = 5 .$$

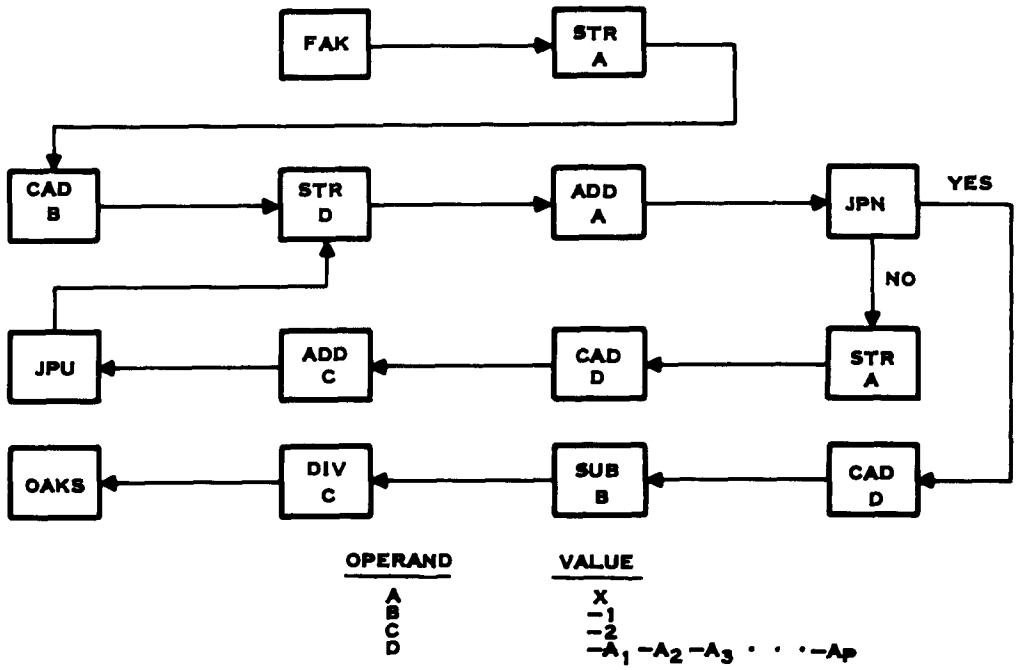
A flow diagram is shown in Figure 47 which illustrates the square-root procedure in terms of machine operations.

The number X is to be entered from the manual control unit. Because the FAK instruction may be used only during the second word time, the first operation is SDN. This is entered on the first line of the Programming Sheet (Figure 44). Note that a zero address must be used here. Arbitrary memory assignments are made for the second instruction line, beginning with A for relative address 0. The entire sequence of operations is now entered in the operation column, with the OAKS operation listed in the last position. Jump operations are supplied as required to extend the jump lengths. SDN operations are supplied as needed to restore a desired memory configuration.

Beginning with the first instruction, the status of the operand memory is determined for each instruction. The first instruction causes the operand memory to shift 0 + 1, or one word. This causes operand A to be in address 1 prior to execution of the first instruction. Note that the memory status shown for each instruction is the status prior to execution of that instruction. The FAK operation does not address the operand memory; therefore, the status of the memory remains unchanged upon execution of the second instruction. As indicated by the flow sheet, the next step is to store in A. The address of A for the third instruction is shown by the Programming Sheet to be 0. The corresponding total memory shift for the third instruction is 0 + 1, or one word. This procedure is repeated until all addresses have been determined. The program has now been completed in mnemonic form and is ready for coding.

The Coding Sheets may be prepared by referring to the machine codes listed in Tables 18 and 19. A completed coding sheet for the example is shown in Figure 45.

The Paper-Tape-Punch Data Sheets may be prepared by referring to the paper-tape formats given in Figure 41. A completed Paper-Tape-Punch Data Sheet for this example is presented in Figure 46.



Square-Root Flow Diagram
Figure 47

The Desk-Calculator Programming Sheet is shown in Figure 48.

6.9 Operating Instructions

6.9.1 General Instructions

A layout of the control panel is shown in Figure 49.

a. Place POWER SWITCH in ON position.

b. Allow 10 seconds for warm-up.

c. Depress CLR button.

d. Place MODE SELECTOR SWITCH in LOAD position.

e. Load memories in either of the following ways:

(1) Automatically, by using the paper-tape reader, in which case the reader is started by depressing the READER START button.

(2) Manually, by using the push-buttons. In this case, an old instruction is erased by depressing the ERA button, and a new instruction is entered bit by bit by means of the bit buttons. The current instruction is displayed

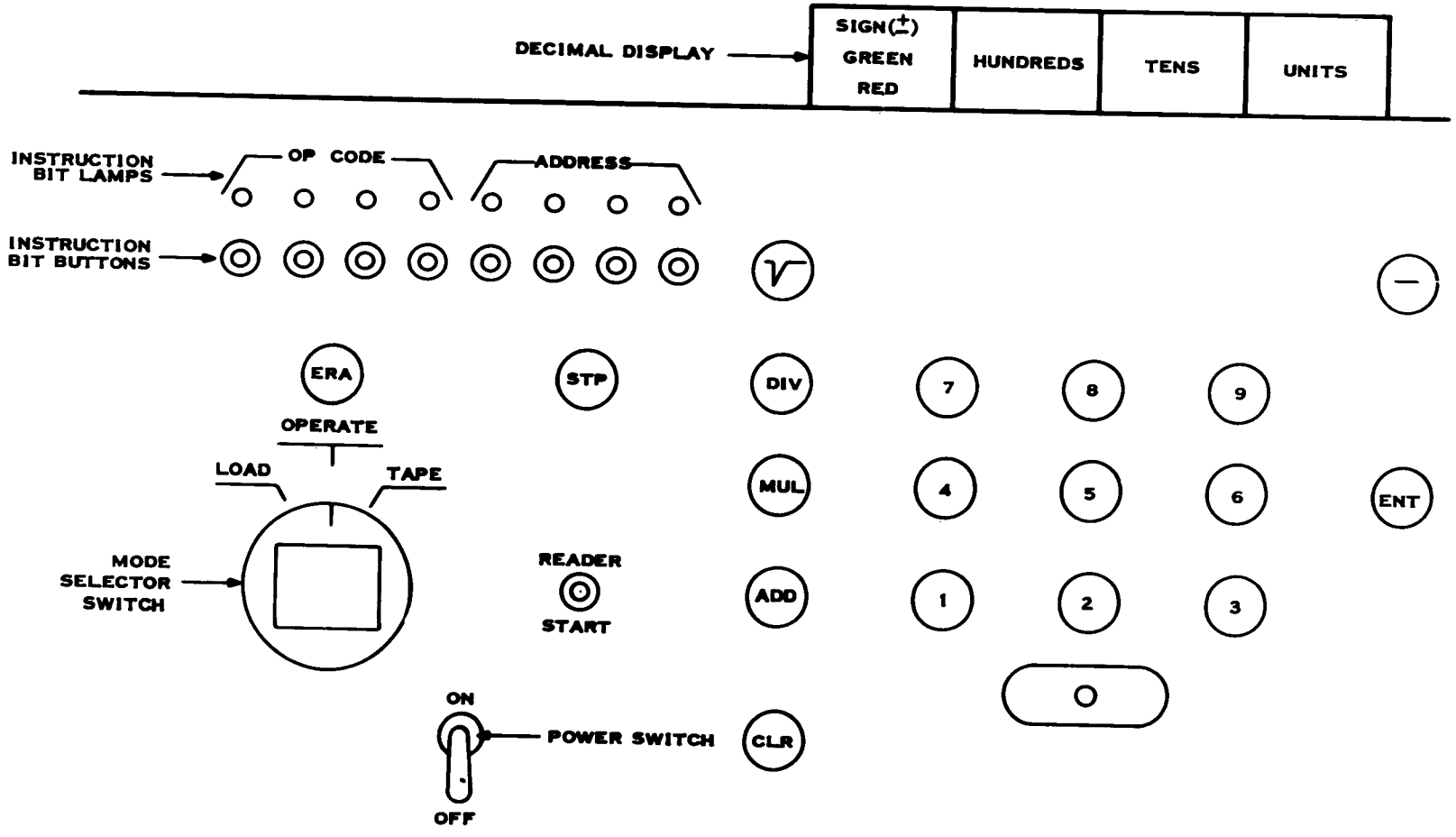
X	
ADD SUB	0
MULT	11
DIV	2
SQ. ROOT	14

PROGRAMMING SHEET
DESK-CALCULATOR PROGRAM

A PREVIOUS RESULT
B −1
C −2
D INITIAL −1 EACH TIME
E WORKING MEMORY

	OPERATION	ADDRESS	INST. NO.	OPERAND RELATIVE ADDRESS															
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INPUT	STR	0	1												E	D	C	B	A
	FAK	—	2	A												E	D	C	B
	JPU	13	3	A												E	D	C	B
MULT	MUL	15	4	A												E	D	C	B
	JPU	10	5	A												E	D	C	B
	JPU	1	6	B	A												E	D	C
	CAD	0	7	A												E	D	C	B
	STR	1	8	B	A													D	C
	ADD	12	9	D	C	B	A												E
SQUARE	JPN	7	10	A												E	D	C	B
	STR	15	11	A												E	D	C	B
	CAD	2	12	A												E	D	C	B
	ADD	14	13	D	C	B	A												E
	SDN	14	14	C	B	A												E	D
	JPU	7	15	B	A												E	D	C
	JPU	14	16	A												E	D	C	B
	JPU	6	17	A												E	D	C	B
	CAD	2	18	A												E	D	C	B
ROOT	SUB	13	19	D	C	B	A												E
	DIV	0	20	B	A												E	D	C
	SDN	13	21	C	B	A												E	D
	JPU	8	22	A												E	D	C	B
	JPU	14	23	B	A												E	D	C
	JPU	X	24	A												E	D	C	B
ADD	ADD	15	25	A												E	D	C	B
	JPU	4	26	A												E	D	C	B
DIV	STR	3	27	A												E	D	C	B
	CAD	11	28	E	D	C	B	A											
	DIV	3	29	A												E	D	C	B
	SDN	11	30	E	D	C	B	A											
OUT	SDN	14	31	A												E	D	C	B
	OAKS	—	32												E	D	C	B	A

Desk-Calculator Programming Sheet
Figure 48



Control Panel
Figure 49

by the bit lamps. Depression of the STP button steps the instruction memory to the next instruction. Operands are loaded by using the 10-digit keyboard, with sign, to set a desired number in the decimal display. When this number appears correctly, it is loaded by depressing the ENT button.

f. Return mode selector switch to the OPERATE position.

g. The computer is started by depressing the ENT button.

h. Tapes may be prepared, using the paper-tape punch, by placing the mode selector switch in the TAPE position.

6.9.2 Special Instructions for Desk-Calculator Program

a. Complete items a—f as prescribed in the General Instructions.

b. Select the desired arithmetic operation by means of the corresponding button. Subtraction is accomplished by addition of negative numbers. The initial operand of a computation sequence must be ADDED to the cleared machine.

c. After selection of an operation, the desired number is set in the decimal display through the use of the decimal digit keys. A number may be made negative in sign, after it has been arrayed, by depressing the (−) button.

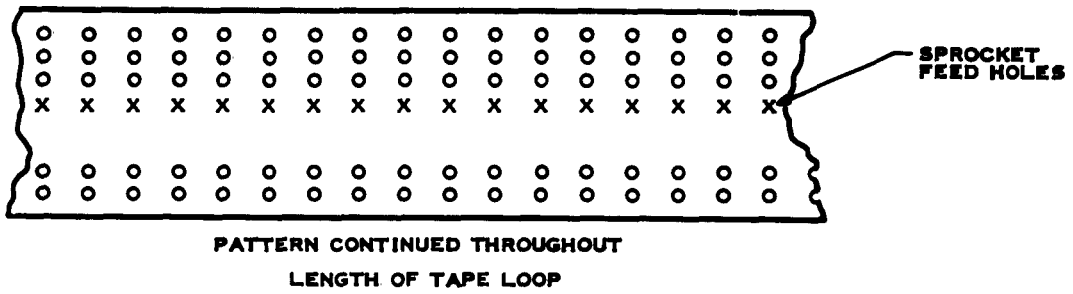
d. The selected operation is executed when the ENT button is depressed. A green background in the sign position of the decimal display indicates that the displayed number has not been entered into the computer. A red background in the sign position indicates that an overflow or a division-by-zero has occurred. When this occurs, the machine should be cleared by depressing the CLR button.

e. After a given arithmetic operation has been selected, the machine will continue to execute that operation, upon depressing the ENT button, until a different operation has been selected. The machine is cumulative; that is, the result of a given computation becomes an operand for the succeeding operation unless the machine is cleared by depressing the CLR button.

EXAMPLE:

$$\text{Find: } \sqrt{\left[\frac{(32)\ (10)}{4} + 1\right]\ (3) - 162}.$$

(1) Complete items a—f in the General Instructions.



Tape Format for Adjustment of Feed Pulse
Figure 50

(2) Manipulate switches in the following sequence:

ADD, 3, 2, ENT, DIV, 4, ENT, MUL, 1, 6, ENT, ADD, 1, ENT, MUL, 3, ENT, ADD, 1, 6, 2, −, ENT, $\sqrt{\ }$, ENT.

The answer is + 15.

6.9.3 Special Instructions for Tape Units

6.9.3.1 Adjustment of Feed Pulse

The tape-reader feed pulse may be adjusted in one of two ways:

a. Place "feed-pulse adjust" tape (Figure 50) in the tape reader, set the mode switch in the LOAD position and press READER START button. The waveform on the white test point can be observed on an oscilloscope and the adjustment potentiometer on card No. 16 can be turned until the waveform shown below is observed.

1.5 to 1.75 msec

b. The tape is loaded and the reader started as above. A 10,000-ohm-per-volt meter (Triplett 630-NA) is used to measure the voltage at the white test point. The adjustment is made to give an output voltage of 0.05 to 0.06 volt.

6.9.3.2 Tape Preparation

a. Operands may be prepared by placing the mode switch in the LOAD position. The operand to be punched is entered into the keyboard and the ENT button pressed.

b. Instructions are prepared by placing the mode switch in the TAPE position. The desired instruction is loaded by pushing the proper instruction-bit buttons and then pushing the ENT button.

c. Tape reproduction can be done by placing the tape to be reproduced in the tape reader, setting the mode switch to the TAPE position and pushing the ENT button for each frame to be reproduced.

6.10 Computer Testing Procedures

Special programs were written to facilitate testing of the computer. Most noteworthy of these were the operand-memory loading program and the arithmetic exercising program.

The operand-memory loading program fills the operand memory continuously with an operand selected from the manual control unit. The program runs until it is halted by depressing the CLR button. This program is particularly useful for finding bad memory stacks. The test operand may be traced throughout the length of the operand memory with an oscilloscope and any errors can be readily observed.

The arithmetic exercising program accepts an input operand, X, from the manual control unit where X is in the range $1 \leq |X| \leq 33$. The operand, X, is stored, multiplied by itself, divided by itself, subtracted from itself, and tested for zero. If it is zero, the process is repeated continuously. If a result other than zero is obtained, the machine stops and displays the erroneous answer in the manual control unit. This program may be halted by depressing the CLR button.

6.11 Fabrication

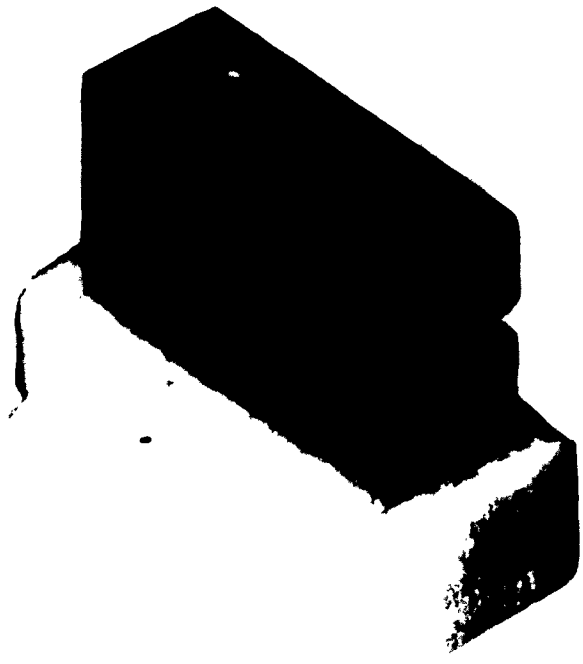
6.11.1 Techniques

Fabrication techniques used in building the computer were described in detail in ASD Interim Reports 7-865 (II) and 7-865 (III).

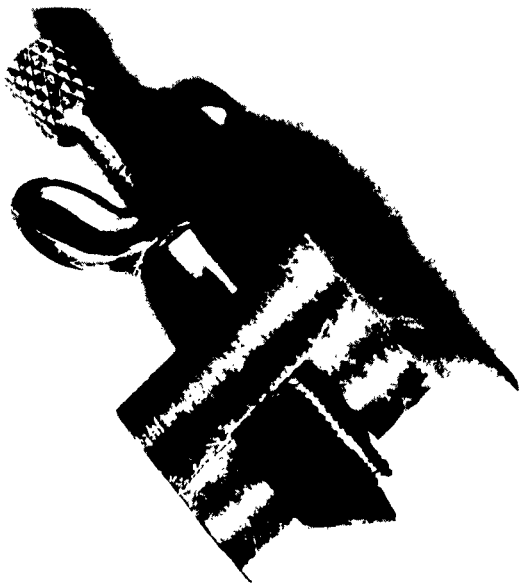
6.11.2 Problems Encountered

Some difficulty has been experienced due to shorts occurring between stack pins and the heat sink frame. The solution to this problem is to provide a wider margin of potting compound around the pin array on the bottom of the stack. This must be done for the second computer.

Air-Turbine Drill In Use
Figure 51



Repaired Stack Before Re-Encapsulation
Figure 52



Extractor Tool
Figure 53

The original thought regarding repair of stacks was that the encapsulant would be dissolved, thereby providing access to the welded assembly. Attempts to remove the encapsulant met with very little success. Repair of defective stacks was finally facilitated through the use of a high-speed, air-turbine drill, similar to the type used in dentistry. The drill is shown in Figure 51. With the drill, a defective network may be exposed and removed. A replacement network may then be installed in its place. A repaired stack is shown in Figure 52, prior to re-encapsulation.

In order to meet the established triggering requirements, the SN209 input capacitors were higher in value than those of the conventional-component computer. The cumulative effect of this was that higher capacitive loads were presented to the gated clock pulse drivers, resulting in deterioration of the gated clock pulses in both memories. This was remedied by a redistribution of the gated clock signals for the memories. Additional drivers, type SN216, were added, as required, to restore the clock waveforms.

The point-to-point wiring which was used for the back-panel wiring produced some congestion which was an impediment to trouble-shooting. Other methods for interconnecting stacks will be investigated for use in the second computer

6.11.3 Stack Removal

It was necessary to provide a means for extracting stacks from the heatsink frame. A special extractor tool was devised to facilitate stack removal (Figure 53). The tool has a screw which fits the threaded extractor hole in the center of the top of the stack. After this screw has been inserted, the stack may be extracted by turning the wing nut on the extractor tool. Figure 54 shows the tool in use.

Extractor Tool in Use
Figure 54

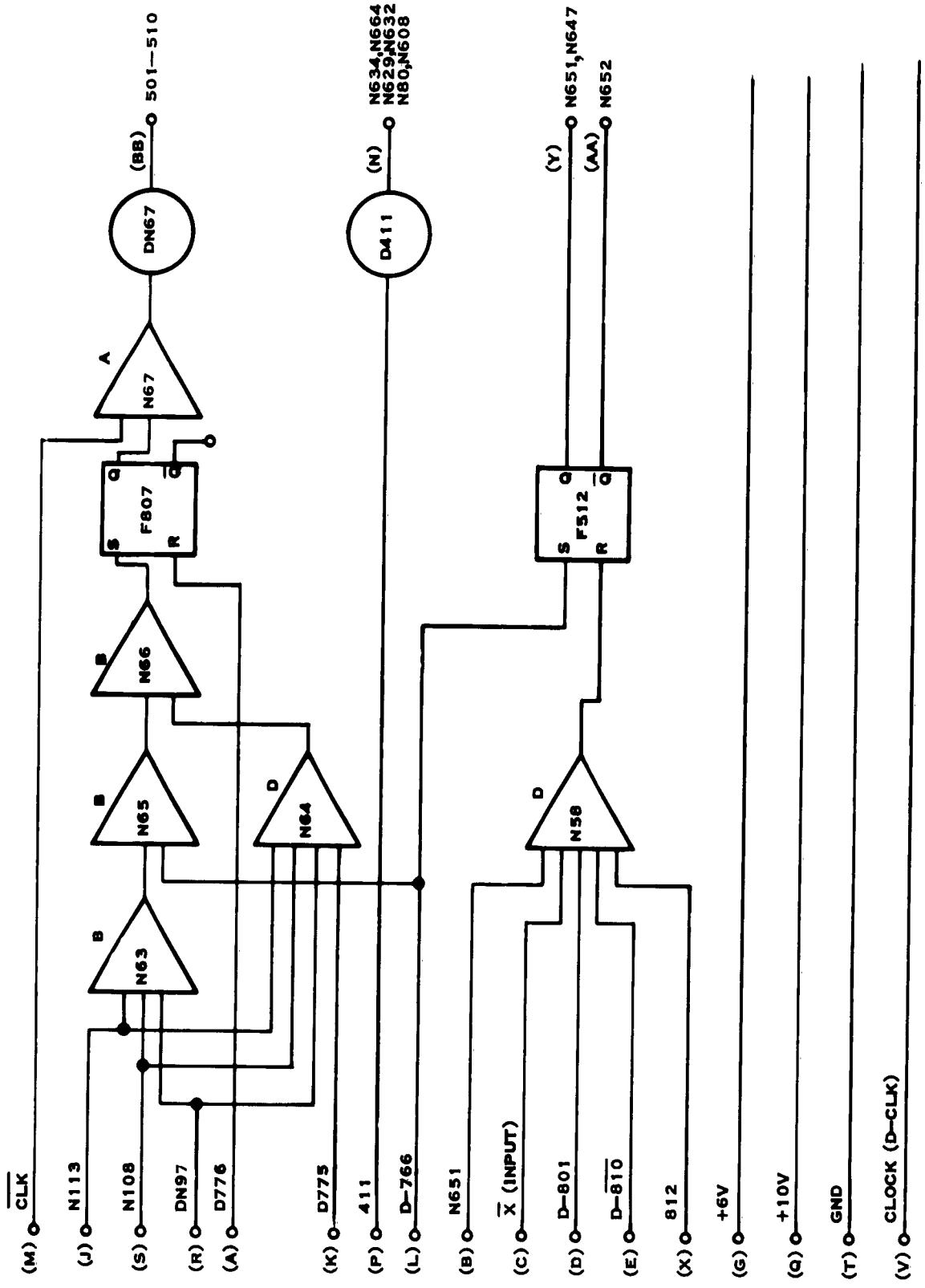
6.11.4 Documentation

Documentation of the semiconductor-network computer stacks consist of two types of information:

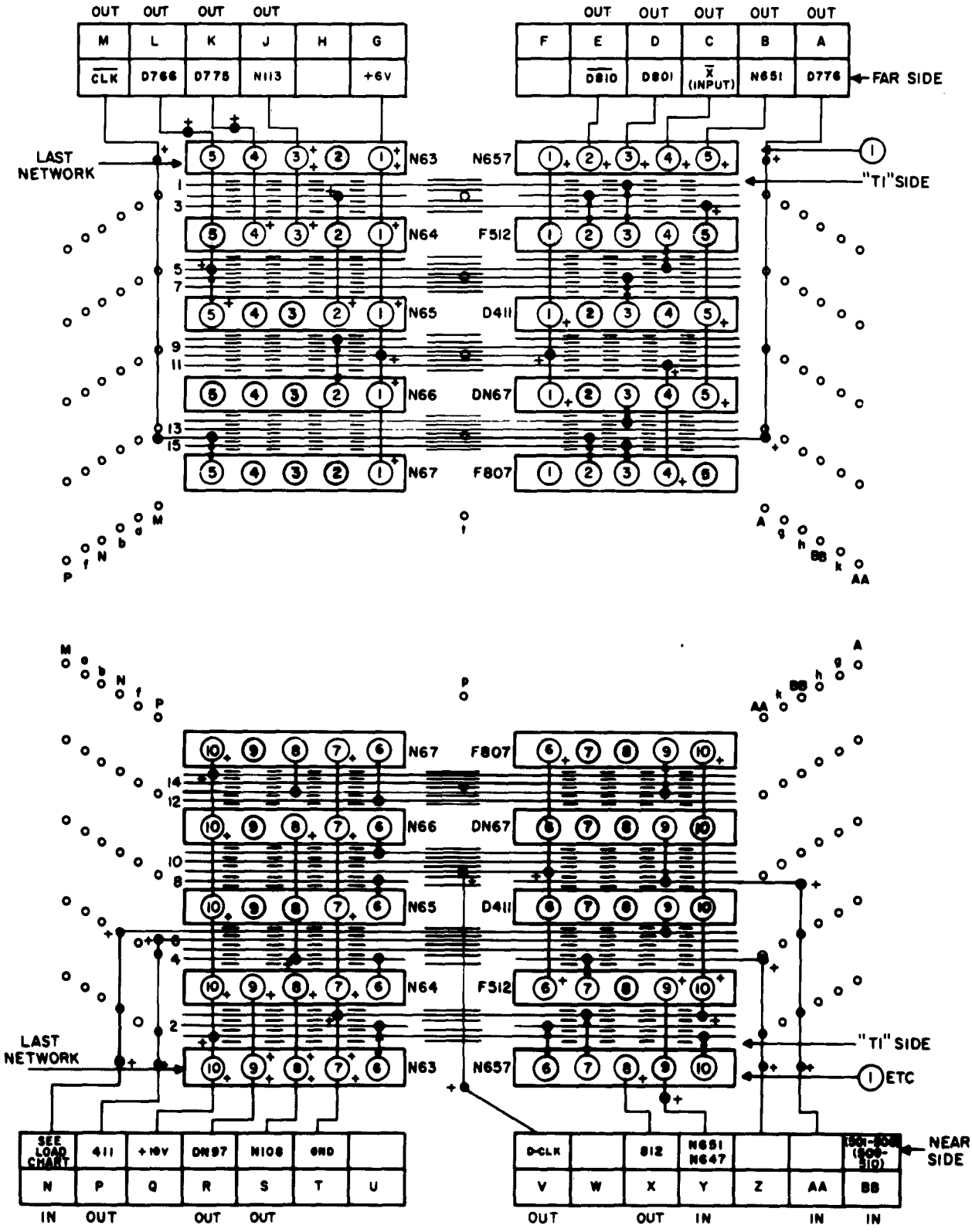
a. Stack logic

b. Stack pictorial wiring diagram.

An example of stack logic is presented in Figure 55, and Figure 56 is a stack pictorial wiring diagram.



Example of Stack Logic
Figure 55



Stack Pictorial Wiring Diagram
Figure 56

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